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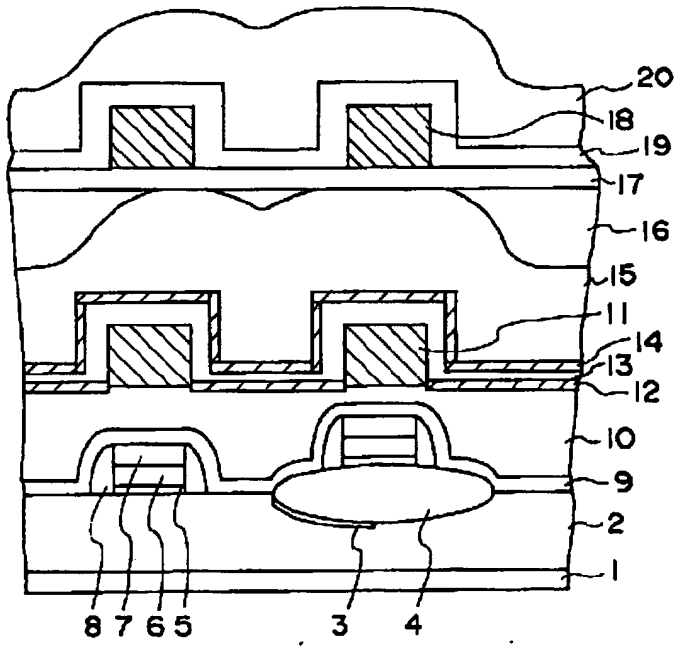
(54) **TITLE OF THE INVENTION:**

Semiconductor device and the method of manufacturing the same

(57) **ABSTRACT**

PROBLEM TO BE SOLVED: To provide a method of manufacturing a semiconductor device wherein the diffusion of moisture is prevented by improving the interlayer film's resistance against water permeability.

SOLUTION: After a metal interconnect 11 is formed, the surface of the substrate is exposed to gas plasma containing the element nitrogen (N). As a result of this exposure to plasma, an insulating film 12 highly resistant to water permeation and containing nitrogen is formed on the surface of a borophosphosilicate glass (BPSG) film 10. Then a P-TEOS film 13 is formed on the substrate surface. Next, an O_3 TEOS film 15 and an SOG film 16 are formed sequentially on the insulating film 14.



CLAIMS

What is claimed is:

1. A method of manufacturing a semiconductor device, comprising:

a first step for forming an interlayer insulating film;

a second step for washing the surface of the interlayer insulating film;

a third step for forming a metal film on the interlayer insulating film;

a fourth step for forming an interconnect by patterning the metal film; and

a fifth step for exposing the surface to nitrogen plasma or gas plasma containing the element nitrogen after the interconnect is formed.

2. A method of manufacturing a semiconductor device, comprising:

a first step for forming an interlayer insulating film;

a third step for forming a metal film on the interlayer insulating film;

a fourth step for forming an interconnect by patterning the metal film; and

a fifth step for exposing the surface to nitrogen plasma or gas plasma containing the element nitrogen after the interconnect is formed.

3. A method of manufacturing a semiconductor device according to claim 1, further comprising a sixth step for forming a contact hole in the interlayer insulating film, and wherein the second step is carried out after the sixth step.

4. A method of manufacturing a semiconductor device according to claim 2, further comprising:

a seventh step for forming a second interlayer insulating film to be carried out after the step 5; and

an eighth step for exposing the second interlayer insulating film to nitrogen plasma or gas plasma containing the element nitrogen.

5. A semiconductor device provided with a functional element and an interlayer insulating film formed on the top layer of the functional element, comprising a silicon oxide film, which is made from SiH_4, N_2O and N_2, located in between the functional element and the interlayer insulating film and formed by plasma-enhanced chemical vapor deposition (CVD) and having a hydrogen

concentration of 1 x 10^{21} to 5 x 10^{22} atoms/cm^3 and a nitrogen concentration of 1 x 10^{21} to 2 x 10^{22} atoms/cm^3.

6. A method of manufacturing a semiconductor, wherein the semiconductor device according to claim 5 is manufactured by forming the silicon oxide film by plasma-enhanced CVD using a gas flow ratio of the flow rate of SiH_4 gas to the sum of the flow rates of N_2O and N_2 gases is within the range of 0.055 to 0.086 .

7. A semiconductor device having a multilevel interconnect structure with the space between adjacent interconnects being insulated by interlayer insulating films, wherein the hydrogen content supplied by Si-H bonds in one layer of the interlayer insulating film is at 5 x $10^{20}/cm^3$ or more, but 5 x $10^{22}/cm^3$ or less.

8. A method of manufacturing a semiconductor device, further comprising a step wherein the interlayer insulating film, having the hydrogen content of its Si-H bonds at 5 x $10^{20}/cm^3$ or more, but 5 x $10^{22}/cm^3$ or less, is formed by vapor deposition using silane gas as the material source.

9. A semiconductor device having a multilevel interconnect structure with the space between the adjacent interconnects insulated by the interlayer insulating films, wherein:

the interlayer insulating film is provided with the first insulating film and the second insulating film formed on the first insulating film and containing, at least, some moisture; and

the hydrogen content of the Si-H bonds of the first insulting film is 5 x $10^{20}/cm^3$ or more, but 5 x $10^{22}/cm^3$ or less.

10. A method of manufacturing a semiconductor device, comprising:

a first step for forming sidewalls on the sides of a gate electrode by etching;

a second step for exposing the entire surface of the semiconductor substrate, including the sidewalls, to fluorine plasma or gas plasma containing fluorine; and

a third step for thermally diffusing the fluorine of the fluorine layer, thus formed on the surface of the side walls by this exposure to plasma, into a gate oxide film by a subsequent heat treatment without removing the fluorine layer.

11. A method of manufacturing a semiconductor device according to claim 10, further comprising a fourth step for removing the etching residue to be carried out after the first step, and wherein the second step carried out after the fourth step.

12. A method of manufacturing a semiconductor device, comprising:

a first step for forming an interlayer insulating film;

a second step for exposing the surface of the interlayer insulating film to fluorine plasma or gas plasma containing fluorine; and

a third step for thermally diffusing the fluorine of the fluorine layer, thus formed on the surface of the interlayer insulating film by this exposure to plasma, into a gate oxide film by a subsequent heat treatment without removing the fluorine layer.

13. A method of manufacturing a semiconductor device, comprising:

a first step for forming an interlayer insulating film;

a second step for forming a contact hole in the interlayer insulating film;

a third step for forming a metal film on the interlayer insulating film;

a fourth step for forming on the metal film a resist for interconnect;

a fifth step for forming an interconnect by patterning the metal film using the resist for the interconnect as a mask;

a sixth step for removing the resist for the interconnect;

a seventh step for exposing the entire surface of the semiconductor substrate to fluorine plasma or gas plasma containing fluorine; and

an eighth step for thermally diffusing the fluorine of the fluorine layer, thus formed on the surface of the interlayer insulating film by this exposure to plasma, into a gate oxide film by a subsequent heat treatment without removing the fluorine layer.

DETAILED DESCRIPTION OF THE INVENTION

[0001]
Technical Field of the Invention: The present invention relates to a semiconductor device having a multilevel interconnect structure and a method of manufacturing the same.

[0002]
Description of Related Art: In a semiconductor device having a metal oxide semiconductor (MOS) transistor whose gate length is less than 1.0 μm, the use of SOG, P-TEOS, or O_3-TEOS films as the film formed on the substrate surface is coming into practice, in order to make flat the surface of the interlayer insulating films, which are used as insulation between the adjacent levels of interconnect. A spin-on glass (SOG) film is formed by spin-coating the surface of the substrate with a solution prepared by dissolving a glass precursor into an organic solvent, whereas a P-TEOS film is an oxide film formed from tetraethyl orthosilicate (TEOS) in plasma. Moreover, a TEOS-O_3 film is an oxide film formed from TEOS and O_3 at atmospheric pressure. However, such plasma-enhanced oxide films or TEOS-O_3 oxide films made from TEOS have very high moisture contents, as is the case with SOG. Consequently, when these film are formed on the interlayer insulating film constituting the top layer of the MOS transistor to make the substrate surface flat, moisture contained in these films is sometimes diffused into the interface of the gate oxide film with the silicon substrate by a subsequent heat treatment. As a result, the moisture forms traps in the gate oxide film. Since these traps capture electrons or other carriers when the transistor is operated, this raised the problem that the lifetime of hot carriers was compromised. Such a problem has been reported, for instance on pages 122 to 126 of the article described below, and it has become a serious issue.

[0003] Since the International Reliability Physics Symposium of 1992, a number of suggestions have been proposed to overcome such a problem, including a first prior art, which was disclosed in JP Application Kokai Publication No. H04-29319. In particular, a finely grained insulator layer is formed on the surface of a porous interlayer insulating film, which, in turn, is formed on the lower electrode, by plasma processing using O_2 or N_2 gas. A contact hole is then formed at the prescribed location of the insulation layer and the interlayer insulating film, to be followed by the vapor deposition of a metal film on the insulator layer. The upper electrode is then formed by patterning the metal film into a prescribed shape. With such a method of manufacturing, the diffusion of moisture to the lower electrode through the interlayer insulating film is prevented by the insulator layer. As a result, leakage between interconnects due to moisture permeation can be prevented. Moreover, the migration of metal atoms from the upper electrode to the lower electrode can also be prevented by the insulator layer, thus suppressing electro migration.

[0004] Moreover, a second prior art, which was disclosed in JP Application Kokai Publication No. H05-55387, was also proposed. More particularly, an SOG film is formed on the surface of the first insulating film, which envelopes the first semiconductor pattern, in order to make its surface flat. The surface of the SOG film is then treated with nitrogen plasma to obtain a nitride layer on its surface. A second insulating film is formed on the nitride layer, and then a via hole,

which penetrates through these films, is formed. Then, a second semiconductor pattern, which is connected to the first semiconductor pattern, is formed on the second insulating film. With such a method of manufacturing, the hygroscopicity of the SOG film is reduced by the nitride layer formed on its surface. As a result, the penetration of moisture from the atmosphere is blocked by the nitride layer. Therefore, when the second conductor pattern fills the via hole, no moisture is released from the SOG film into the interior wall of the via hole, and the metal used for sputtering adheres properly to the wall surface of the via hole.

[0005] A third prior art is also disclosed in JP Application Kokai Publication No. H05-55387. To described it in more detail, after the surface of the first insulating film covering the first semiconductor pattern is made flat by the SOG film, a second insulating film is formed on it, and then a via hole is formed through these films. Then, the surface of the substrate is exposed to nitrogen plasma to form a nitride layer on the face of the SOG exposed on the interior wall of the via hole and on the surface of the second insulating film. A second semiconductor pattern is then formed on top of the layer thus obtained. With such a method of manufacturing, moisture in the SOG film is reduced by the heat of the processing with nitrogen plasma, and the nitride layer, which blocks moisture diffusion, is also formed on the interior wall of the via hole and on the surface of the second insulating film. With a result that the metal film is adhered faultlessly to the interior wall of the via hole, because no moisture is released there.

[0006] Moreover, there has been a report of a technique wherein the degradation of hot carriers is controlled through the prevention of water diffusion achieved by means of a P-SiO film formed on the gate oxide film. Here, the P-SiO film is a silicon oxide film formed from SiH_4 by plasma-enhanced CVD.

[0007] A fourth prior art, which was disclosed in JP Application Kokai Publication No. S62-145735, proposed a method of manufacturing this P-SiO film from SiH_4, N_2O and N_2. With this method, the silicon oxide film is formed using the gas infusion rate of 18 sccm for the SiH_4 gas, 3 sccm for the N_2O gas and 150 sccm for the N_2 gas.

[0008] According to a fifth prior art, which was disclosed in JP Application Kokai Publication No. H01-186627, moreover, N_2 is not used in the proposed method to improve the quality of the insulating film. Instead, the method uses the gas infusion ratio of $SiH_4 / N_2O \geq 0.1$ to form a P-SiO film for this purpose.

[0009] According to the method proposed by a sixth prior art, which was disclosed in JP Application Kokai Publication No. H03-151654, moreover, a P-SiO film having a nitrogen concentration of 5 mole% or higher is formed from SiH_4, N_2O and N_2 in between the SOG film and the aluminum interconnect. As a result, the diffusion of mobile ions present in the SOG film is blocked by the P-SiO film.

[0010] According to the method proposed by a seventh prior art, which was disclosed in JP Application Kokai Publication No. H02-128424, moreover, a silicon oxide film, whose composition is such that it has an oxygen-to-silicon mole ratio of 2 to 1, is provided in between

the hydrogen-generating insulating film and the circuit element. Since such a silicon oxide film has a high dangling-bond content, the diffusion of hydrogen from the SOG or P-SiN film can be prevented.

[0011] According to the method proposed by an eighth prior art, which was disclosed in JP Application Kokai Publication No. H05-166936, moreover, the diffusion of hydrogen from the SOG is prevented by raising the nitrogen content of the silicon oxide film to 2.4 atomic% or more.

[0012] Moreover, JP Application Kokai Publication No. H04-218947 presented a method wherein the effects on the device was reduced by providing an SiO_2 film of a low film-density and by releasing the mobile ions and the like of the SOG film in the opposite direction to that of the semiconductor element. According to the method presented by a ninth prior art, which was disclosed in JP Application Kokai Publication No. H03-151654, moreover, the diffusion of the mobile ions and the like in the SOG film towards the semiconductor element was prevented by raising the nitrogen content of the SiO_2 film to a level of 5 mole% or more.

[0013] Furthermore, the aforementioned document, *International Liability Physics Symposium*, described a serious problem that moisture diffused into the gate oxide film during heat processing shortens the lifetime of hot carriers. A technique used to improve the hot-carrier tolerance using fluorine has been reported to overcome this problem, as demonstrated in page 1,426 of the document below.

[0014] According to a report in the *IEEE Transactions on Electron Devices*, 1990, Vol. 3, Issue 6, the technique disclosed was used to improve hot-carrier tolerance by terminating the dangling bonds of silicon with fluorine by implanting fluorine ions into the gate. While the bond energy of Si-H bonds is 318 kJ/mol, that of Si-F bonds is 591 kJ/mol. In other words, because the bond energy of Si-F bonds is close to 622 kJ/mol, which is the bond energy of Si-O bonds, bonds obtained by terminating silicon dangling bonds with fluorine are less likely to be severed when hot carriers are injected than those obtained by terminating the dangling bonds with hydrogen. Therefore, using fluorine to terminate dangling bonds results in improved hot-carrier tolerance. However, because fluorine ions are implanted into the entire surface of the gate insulating film in this case, fluorine is present throughout the entire channel region. Consequently, the gate oxide film becomes thicker, and the gate capacitance is reduced, thereby causing a reduction in the driving current value of the MOS transistor. This is a disadvantage.

[0015] In order to overcome this problem, JP Application Kokai Publication No. H03-296270 proposed a method wherein an oxide film is first formed on a polysilicon gate and fluorine ions are implanted from above. With this method, however, manufacturing cost is higher because the number of steps must be increased in order to carry out the implantation with fluorine ions.

[0016] JP Application Kokai Publication No. H04-62974 proposed a method wherein heat treatment is carried out in an environment containing halogen after the gate electrode is formed. With this method, however, because the fluorine interfused into the oxide film, which forms the

channel section, through all of its sectional surfaces causes the thickening of the oxide film, the gate capacity is decreased, thus causing the problem of a reduced driving current value of the MOS transistor.

[0017] In JP Application Kokai Publication No. H01-230239, a method was proposed for diffusing fluorine by the interfusion of fluorine gas during the process of forming the interlayer insulating film. However, the interfusion of large quantities of fluorine used in this method means that large quantities of fluorine are mixed into all parts of the gate oxide film, which is to serve as the channel section. Consequently, the oxide film [thickness] is increased, while the gate capacitance is reduced, resulting in a reduced driving current value of the MOS transistor.

[0018] Consequently, methods involving ion implantation or treatment in a fluorine-series gas environment cannot be put to practice because they have the effect of reducing the driving capacity of the MOS transistor. A method wherein the diffusion of fluorine into the gate oxide film is achieved by exposing the semiconductor substrate surface to fluorine plasma or gas plasma containing fluorine is also conceivable as a method of terminating the dangling bonds of silicon with fluorine by introducing fluorine into the gate oxide film. Fluorine plasma or gas plasma containing fluorine is also used for etching.

[0019] According to a tenth prior art, which was disclosed in JP Application Kokai Publication No. H01-217919, for example, the proposed method removes reactive products generated during the processing of the gate electrode by first carrying out gate etching using a fluorine-series gas, and then by washing with hydrofluoric acid, after exposure to oxygen plasma.

[0020] Moreover, an eleventh prior art, which was disclosed in JP Application Kokai Publication No. H02-139932, proposes a method that uses a sample whose first conductor layer is comprised of the part that is not covered by the insulating film formed on it. With this method, after exposure to gas plasma containing halogen atoms, a second conductor layer is formed. In this manner, the carbon compounds and the like adhering to the first conductor layer are removed, and the second conductor layer is allowed to be deposited to completion by chemical vapor deposition.

[0021] Moreover, according to a method proposed by a twelfth prior art, which was disclosed in JP Application Kokai Publication No. H03-157931, a resist is provided with a water repellent property by exposing the patterned resist to fluorine plasma. Then the silicon compounds are allowed to react with water in vapor, a silicon oxide film is formed on parts not covered by the resist, and after the resist is removed, a plasma oxide film is formed, to obtain a flat surface that is not dependent on a pattern.

[0022] Furthermore, with the method proposed by a thirteenth prior art, which was disclosed in JP Application Kokai Publication No. H05-102108, after the contact hole is formed and the resist is subjected to ashing using gas containing fluorine and oxygen, the resist is removed with an organic solvent.

[0023] Further still, a method proposed by a fourteenth prior art, which was disclosed in JP Application Kokai Publication No. H05-267157, uses an ashing method in which the resist patterned on the interconnect is subjected to ashing using gas such as $O_2/CHF_3/CH_3$ OH.

[0024]
Problems to be Solved by the Invention: In the first prior art, which was disclosed in JP Application Kokai Publication No. H04-29319, however, the surface of the substrate is normally washed with buffered fluoric acid (BHF) before the surface of the plasma oxide film is covered with a metal film, which is used to form the upper electrode, by vapor deposition. Consequently, the plasma insulating film on the substrate surface is made thinner by this treatment with BFH. Moreover, after the metal film, which is intended for the upper electrode, is formed, the plasma insulating film lying under the metal film is stripped further by the etching process used to pattern the metal film. As a result, the effectiveness of the plasma insulating film in blocking the diffusion of moisture and the like is reduced. Consequently, the diffusion of water cannot be prevented when an insulating film with a high moisture content such as a P-TEOS, O_3-TEOS or SOG film is to be formed on top. This is the reason that the use of such films for the MOS transistor causes the diffusion of the moisture into the gate oxide film, thereby accelerating the degradation of the lifetime of hot carriers.

[0025] Moreover, in the case of the second prior art, which was disclosed in JP Application Kokai Publication No. H5-55387, wherein a nitride layer is formed on the surface of the SOG film by nitrogen-plasma processing, the diffusion of the moisture from the atmosphere into the layer under the nitride layer can be prevented. However, if the SOG film is formed on top of an insulating film with a high moisture content such as a P-TEOS, O_3-TEOS or SOG film, then it means that the moisture present in such a film penetrates into the lower layer by diffusion. Furthermore, the diffusion of the water present in the SOG film itself cannot be prevented. As a result, when an MOS transistor is formed under such a layer, this moisture is also diffused into the gate oxide film to generate traps, thereby shortening the lifetime of hot carriers.

[0026] Moreover, the third prior art, which was disclosed also in JP Application Kokai Publication No. H05-55387, wherein a nitride layer is formed on the internal wall of the via hole and on the surface of the second insulating film, poses a problem similar to the one associated with the aforementioned prior art, which was disclosed in JP Application Kokai Publication No. H04-29319, when the second conductor pattern is formed on the surface of the second insulating film. In other words, the nitride layer formed on the substrate surface is made thinner by BHF treatment carried out prior to the forming of the metal film, which is to be used for forming the second conductor pattern. Moreover, the nitride layer is stripped off even further by the etching process used to make the second conductor pattern. As a result, the effectiveness of the nitride layer in blocking the diffusion of moisture and the like is reduced, thus posing a similar problem.

[0027] Furthermore, in the case of the prior art, wherein the degradation of hot carriers is suppressed by preventing the diffusion of water by means of a gate oxide film formed on the P-SiO film, the mechanism by which the P-SiO film prevents the diffusion of water is not yet understood. For this reason, depending upon the conditions of film formation or the film

thickness, it is not possible to prevent the diffusion of water, so the degradation of hot carriers cannot be suppressed.

[0028] In other words, even if an attempt were to be made to prevent the diffusion of moisture into the gate section by means of a P-SiO film, which is obtained by the fourth prior art, placed in the top layer of an MOS transistor, the effects thus obtained would not be sufficient to prevent the diffusion of moisture. As a result, the hot-carrier tolerance of the MOS transistor is compromised. It is thought that this is caused by the inappropriate infusion ratio of each material gas used during the forming of the P-SiO film.

[0029] Further still, even when a P-SiO film obtained according to the fifth prior art without the use of nitrogen is used to serve as a barrier film against moisture diffusion, the diffusion of water cannot be prevented. It is thought that the following is responsible for this: because the P-SiO film of the fifth prior art is formed without using nitrogen, it has a low nitrogen concentration, and Si-N and Si-NH bonds are not found in sufficient quantities on the surface of the insulating film.

[0030] Furthermore, even when a P-SiO film, which is obtained according to the sixth prior art and contains a nitrogen concentration of 5 mole% or higher, is used to serve as a barrier film against moisture diffusion, the diffusion of water cannot be prevented. The reason for this is considered to be as follows: the nitrogen concentration of only 5 mole% or more is not sufficient to prevent the diffusion of water, and Si-H bonds must also be present on the surface of the insulating film if it were to effectively prevent the diffusion of water. Moreover, the JP Application Kokai Publication proposing the sixth prior art described an example wherein a P-SiO film was formed under the conditions of the SiH_4 to N_2O flow rate ratio of 0.05, but merely states "a prescribed quantity" for N_2. Therefore, it is not possible to be specific about this quantity. In other words, with the sixth prior art, it is not possible to be specific about the P-SiO film that is capable of preventing the diffusion of water in a sufficient manner.

[0031] Moreover, even when a silicon oxide film, which is obtained according to the seventh prior art and contains dangling bonds, is used as a barrier film against moisture diffusion, the diffusion of water cannot be prevented. The reason for this is: whereas the concentration of dangling bonds present in the silicon oxide film obtained by a commonly used film-formation method is in the order of 10^{19} spins/cm^3, that of hydrogen in the SOG film is in the order of 10^{21} [atoms]/cm^3, so the hydrogen concentration of SOG film is normally higher than the concentration of dangling bonds in the silicon oxide film. As a result, hydrogen cannot be captured by the dangling bonds in the oxide film.

[0032] Furthermore, even when a P-SiO film obtained according to the eighth prior art and having a nitrogen content of 2.4 atomic% or more is used as the film to prevent moisture diffusion, it is not possible to totally prevent the diffusion of water. The nitrogen content of merely 2.4 atomic% or more is not enough to prevent the diffusion of water, and the concentration of Si-H bonds must be at a value within a prescribed range. Moreover, because the P-SiO film is made from only SiH_4 and N_2O, the formation of Si-NH bonds in the film is not

sufficient unless N_2 is also used, and the diffusion of water from the SOG and O_3-TEOS films cannot be totally prevented.

[0033] Moreover, with advances in the microminiaturization of devices, the performance of semiconductor devices with respect to mobile ions is tending to be more often compromised. As a result, if an SOG film is used, then it becomes necessary to form a plasma oxide film, which has the effect of suppressing the diffusion of mobile ions and the like from the SOG film. A method of forming a plasma oxide film, which has the effect of suppressing the diffusion of mobile ions and the like from the SOG film, was presented by the ninth prior art, which was disclosed in JP Application Kokai Publication No. H03-151654. According to this method, a plasma oxide film having a nitrogen content of 5% or more is formed by means of a parallel-plane plasma CVD apparatus using SiH_4, N_2O, and N_2. However, a detailed investigation of the film quality of plasma oxide films was conducted, and the results thus obtained demonstrated that a nitrogen-free plasma oxide film capable of suppressing the diffusion of mobile ions and the like can be formed from monosilane gas and oxygen. Therefore, the present invention provides a semiconductor device that is effective in suppressing the diffusion of mobile ions, water and the like and uses a nitrogen-free plasma oxide film and a method of manufacturing the same.

[0034] Moreover, there is the aforementioned tenth prior art, which was disclosed in JP Application Kokai Publication No. H01-217919, wherein an attempt was made to improve hot-carrier tolerance by diffusing fluorine into the gate oxide film. With this method, the silicon dangling bonds present in the gate oxide film cannot be terminated with fluorine, because fluorine remaining on the gate is also removed during the procedure used to remove reaction products.

[0035] Furthermore, in the case of the eleventh prior art, which was disclosed in JP Application Kokai Publication No. H02-139932, the oxide film into which fluorine has been interfused is stripped away when the interconnect is patterned by etching the second conductor layer. Therefore, it is not possible to diffuse fluorine into the gate oxide film in order to terminate the silicon dangling bonds with fluorine.

[0036] Moreover, in the case of the twelfth prior art, which was disclosed in JP Application Kokai Publication No. H03-157931, as long as washing is not carried out prior to the forming of a silicon oxide film in between metal interconnects by allowing the water to react with silicon compounds in a gaseous environment, fluorine is present because it has not been stripped off by washing. If washing is carried out prior to the reaction of silicon with water in a gaseous environment, however, an insulating film containing fluorine is not obtained. Even though fluorine is allowed to remain if washing is not carried out, this method is not normally used for the flattening process because of its high cost due to increased number of steps required after the interconnect is formed. Normally, the second interlayer insulating film is formed directly on top of or in between the metal interconnects. In this case, the oxide film containing fluorine is taken off when the resist is removed.

[0037] There is also a method according to the thirteenth prior art, which was disclosed in JP Application Kokai Publication No. H05-102108. Again, the oxide film containing fluorine is lost with this method, when the resist is removed with an organic solvent.

[0038] In the case of the method according to the fourteenth prior art, which was disclosed in JP Application Kokai Publication No. H05-267157, moreover, if the oxide film is to be formed on the interconnect after the removal of the resist by ashing, then washing is carried out prior to this. This means that the oxide film containing fluorine is removed during this process.

[0039] The object of the present invention is to overcome these issues by providing a method of manufacturing a semiconductor device, wherein the diffusion of moisture and the like can be prevented by improving the resistance of the interlayer film against water permeation. If a method of manufacturing such a semiconductor device is made available, this will make it possible to create an MOS transistor having a sufficient hot-carrier tolerance to be put to practical use.

[0040]
Means for Solving the Problems: In order to achieve this objective, the present invention was provided with a first step for forming an interlayer insulating film, a second step for washing the surface of the interlayer insulating film, a third step for forming a metal film on the interlayer insulating film, a fourth step for forming an interconnect by patterning the metal film, and a fifth step for exposing the element to nitrogen plasma or gas plasma containing nitrogen after the interconnect is formed.

[0041] Moreover, the present invention was provided with a first step for forming an interlayer insulating film, a third step for forming a metal film on the interlayer insulating film, a fourth step for forming an interconnect by patterning the metal film, and a fifth step for exposing the entire surface to nitrogen plasma or gas plasma containing nitrogen after the interconnect is formed.

[0042] Furthermore, the present invention was further provided with a sixth step for forming a contact hole in the interlayer insulating film after the first step, with the second step carried out after the sixth step.

[0043] Moreover, the present invention was further provided with a seventh step, which is carried out after the fifth step, for forming a second interlayer insulating film and an eighth step for exposing the second interlayer insulating film to nitrogen plasma or gas plasma containing nitrogen.

[0044] Moreover, a semiconductor device provided with a functional element and an interlayer insulating film formed thereon was further provided with a silicon oxide film formed in between the functional element and the interlayer insulating film made from SiH_4, N_2O_2 and N_2 by plasma-enhanced CVD and having a hydrogen concentration of 1×10^{21} to 5×10^{22} atoms/cm^3 and a nitrogen concentration of 1×10^{21} to 2×10^{22} atoms/cm^3.

[0045] With the present invention, the above semiconductor device is manufactured by forming the silicon oxide film by plasma-enhanced CVD using a gas flow rate for SiH_4 so that its gas flow ratio with respect to the sum of the gas flow rate of N_2O_2 and N_2 gases is in the range of 0.055 to 0.086.

[0046] Moreover, the present invention includes a means for forming an insulating film having an oxide-film structure constituting a plasma oxide film, which is made from silane gas with the hydrogen content supplied by Si-H bonds at $5 \times 10^{20}/cm^3$ or more but $5 \times 10^{22}/cm^3$ or less.

[0047] Moreover, the present invention was also provided with: a step for forming sidewalls on the sides of the gate electrode by etching; a second step for exposing the entire surface of the semiconductor substrate, including the sidewalls, to fluorine plasma or gas plasma containing fluorine; and a third step for thermally diffusing into the gate oxide film the fluorine of the fluorine layer, which was formed on the surface of the sidewalls by exposure to plasma, by heat treatment without removing the fluorine layer.

[0048] The present invention was further provided with a fourth step for removing the residue of the etching after the first step, with the second step carried out after the fourth step.

[0049] Moreover, the present invention was provided with: a first step for forming an interlayer insulating film; a second step for exposing the surface of the interlayer insulating film to fluorine plasma or gas plasma containing fluorine; and a third step for thermally diffusing, by heat treatment, fluorine of the fluorine layer thus formed on the surface of the interlayer insulating film without removing the fluorine layer.

[0050] Moreover, the present invention was provided with: a first step for forming an interlayer insulating film; a second step for forming a contact hole in the interlayer insulating film; a third step for forming a metal film on the interlayer insulating film; a fourth step for forming a resist for interconnect on the metal film; a fifth step for forming an interconnect by patterning the metal film using the resist for interconnect as a mask; a sixth step for removing the resist for interconnect; a seventh step for exposing the entire surface of the semiconductor substrate to fluorine plasma or gas plasma containing fluorine; and an eighth step for thermally diffusing into the gate oxide film, by heat treatment, the fluorine of the fluorine layer thus formed on the surface of the interlayer insulating film without removing the fluorine layer.

[0051]
Operation: An insulating film, which is highly resistant to water permeation so that it virtually blocks the permeation of water and contains nitrogen, is formed on the exposed surface of the interlayer insulating film lying in between the interconnect by exposing the surface of the interlayer insulating film to gas plasma containing the element nitrogen after the interconnect is patterned during the fifth step. Consequently, during the second step, in which the surface of the interlayer insulating film is subjected to washing treatment prior to the forming of the metal film, the nitrogen-laced insulating film is not yet formed. Therefore, the nitrogen-laced insulating film, which is highly resistant to permeation of water, is not stripped away by the washing

treatment. Moreover, during the fourth step, in which the metal film is patterned to form the interconnect, the nitrogen-laced insulating film, which is highly resistant to permeation of water, is not stripped away by this patterning process because the film has not been formed at this stage.

[0052] Moreover, during the eighth step, a nitrogen-laced insulating film, which is highly resistant to permeation of water, is also formed on the surface of the second interlayer insulating film when the latter is exposed to gas plasma containing nitrogen.

[0053] Furthermore, the present invention is provided with a silicon oxide film, which is formed in between the functional element and the interlayer insulating film, and which is made from SiH_4, N_2O_2 and N_2 by plasma-enhanced CVD and has a hydrogen concentration of 1×10^{21} to 5×10^{22} atoms/cm^3 and a nitrogen concentration of 1×10^{21} to 2×10^{22} atoms/cm^3. This means that the water that has permeated into the silicon oxide film reacts with Si-H, Si-NH and Si-N bonds present to produce a silicon oxide film. As a result, the diffusion of water present in an SOG or O_3-TEOS film, as well as the drifting of hydrogen away from the silicon oxide film itself, is prevented by this silicon oxide film.

[0054] Moreover, the present invention is provided with an insulating film having an oxide-film structure comprised of a plasma oxide film having a hydrogen content, which is supplied by Si-H bonds, at 5×10^{20}/cm^3 or more but 5×10^{22} /cm^3 or less, and this suppresses the diffusion, into the substrate, of matters such as mobile ions and water present in the film. Although the mechanism whereby the diffusion of water and the like is blocked is not understood, it is presumed that the diffusion of water is blocked by some form of reaction, e.g., in the case of water, $2Si\text{-}H + H_2O \rightarrow Si\text{-}O\text{-}Si + 2H_2 \uparrow$.

[0055] Moreover, the sidewalls of the gate electrode are usually dry-etched in a gaseous mixture of Ar and a fluoride such as CHF_3 or CF_4. However, because the resulting fluoride substance is discharged into the atmosphere, not much remains on the sidewalls. Consequently, fluorine is interfused into the sidewalls by exposing the entire surface of the semiconductor substrate to fluorine plasma or gas plasma containing fluorine after the sidewalls are etched, followed by heat treatment to diffuse the fluorine into the gate oxide film. Silicon dangling bonds are terminated with fluorine by diffusing fluorine into the gate oxide film in this manner.

[0056] Moreover, exposing the surface of the interlayer insulating film to fluorine plasma or gas plasma containing fluorine and then carrying out heat treatment would also result in the diffusion of fluorine into the gate oxide film.

[0057] Moreover, in instances wherein a contact hole is formed in the interlayer insulating film using a gaseous mixture of Ar and a fluoride such as CHF_3 or CF_4, fluorine is not interfused into the entire surface of the semiconductor substrate because the contact hole is etched selectively. Furthermore, the oxide film and the residue from etching found on the surface of the silicon substrate are usually removed subsequently by washing. Consequently, fluorine does not remain in the interlayer insulating film when the contact hole is formed. Moreover, the fluorine-laced oxide film layer is stripped away when the metal film is patterned by etching. Furthermore, the

oxide film layer containing fluorine is also stripped away when the resist is removed by ashing or washing. In these instances, fluorine is diffused into the gate oxide film by exposing the entire surface of the semiconductor substrate to fluorine plasma or gas plasma containing fluorine after the resist is removed and then by carrying out the next step, without first removing the fluorine of the interlayer insulating film.

[0058]
Description of the Preferred Embodiments: A first preferred embodiment of the present invention as applied to the manufacture of a complementary metal-oxide semiconductor (CMOS) will be described hereinafter. Fig. 1 is a cross-sectional view of a semiconductor device obtained by a manufacturing method according to the present embodiment, while Figs. 2 to 5 are cross-sectional views illustrating the manufacturing method of the present embodiment. Although a CMOS is built by combining the n-type MOS and the p-type MOS, only the n-type MOS is shown in these diagrams.

[0059] Firstly, as shown in Fig. 2, the surface of a p-type silicon substrate 1 is oxidized to form a silicon oxide film with a thickness of about 500 angstroms. Then, a p-well 2 is formed by implanting boron ions through the silicon oxide film in the region where an n-type MOS is to be formed using a dose of about 1.2×10^{13} /cm^2. Phosphate ions are implanted into the region where a p-type MOS is to be formed using a dose of around 1.35×10^{13} /cm^2, to form an n-well not shown in the diagram. The implanted boron and phosphate are then diffused by heat treatment to enlarge each well region. Next, after the silicon oxide film on the substrate surface is etched, a pad oxide film is formed on the substrate surface. A silicon nitride film is then formed on the pad oxide film by the chemical vapor deposition (CVD) method. The silicon nitride film in the inactive region where the transistor is not to be formed is removed selectively, leaving behind the silicon nitride film in the active region where the transistor is to be formed. A channel stopper 3 is then formed by selectively implanting channel-stopper ions into the inactive region of the p-type silicon substrate 1. A 6,000-angstrom thick silicon oxide film 4 for isolating the element is formed in the inactive region by thermal oxidation to provide insulation between elements.

[0060] Boron fluoride ions are then implanted into the active region using a dose of around 2.7×10^{12} /cm^2 for the threshold value adjustment. Then, after the pad oxide film is removed by wet-etching, a gate oxide film 5 consisting of a silicon oxide film is formed on the exposed well region, and then a polysilicon film 6 is formed on the gate oxide film 5 by CVD. The resistance of the polysilicon film 6 is then reduced by doping it with phosphate. A tungsten silicide film 7 is then formed by sputtering. After this, the tungsten silicide film 7, the polysilicon film 6 and the gate oxide film 5 are selectively etched to yield a gate electrode.

[0061] Phosphate ions are then implanted on the entire surface of the p-well 2 using a dose of around 2.0×10^{13} /cm^2, while boron fluoride ions are implanted on the entire surface of the n-well, not shown in the diagram, using a dose of around 5.0×10^{12} /cm^2. Next, after a silicon oxide film is formed on the substrate surface by CVD, sidewalls 8 are formed on all sides of the gate electrode by etching back the silicon oxide film. Arsenic ions are then implanted into the p-

well 2 region at a dose of around 3 x 10^{15} /cm^2, whereas boron fluoride ions are implanted into the n-well region, not shown in the diagram, using a dose of around 1.5 x 10^{15} /cm^2. These two ion implantations results in the formation of a source region and a drain region, each of which has a lightly doped drain (LDD) structure, not shown in the diagram.

[0062] Next, a silicon oxide film 9 is formed on the entire surface of the substrate at a low temperature, to be followed by the formation of a silicon oxide film containing boron and phosphorus (BPSG film: boro-phospho-silicate glass film) 10 on the silicon oxide film 9. Heat treatment is then carried out at 900°C for 15 minutes to make the surface of the BPSG film 10 flat. Then the BPSG film 10 and the silicon oxide film 9 lying underneath it are selectively etched to create a contact hole extending to the source and the drain regions, not shown in the diagram, of the transistor. Then, after the substrate surface is washed by treatment with BHF, an aluminum (Al) alloy film is formed on the entire surface of the substrate by sputtering. A desired metal interconnect 11 is then formed by patterning the Al alloy film into a prescribed shape (see Fig. 2).

[0063] Next, after the metal interconnect 11 is formed, the substrate surface is exposed to a nitrogen gas (N_2) plasma or gas plasma containing nitrogen (N), ammonium gas (NH_3), for example, (see Fig. 3). As a result of the exposure to this gas plasma containing nitrogen, a nitrogen-laced insulating film 12 having a high resistance to water permeation is formed on the surface of the BPSG film 10, as shown in Fig. 4. A P-TEOS film 13 is then formed on the substrate surface. Next, the substrate surface is repeatedly exposed to gas plasma containing nitrogen such as ammonia gas or nitrogen gas (see Fig. 4). Ammonia plasma was used in the present embodiment. As a result of these exposures to plasma, a nitrogen-laced insulating film 14 having a high resistance against water permeation is formed on the surface of the P-TEOS film 13, as shown in Fig. 5. Next, an O_3-TEOS film 15 and an SOG film 16 are formed on the insulating film 14 in succession, and then the substrate surface is made flat by etching the SOG film 16 (see Fig. 5).

[0064] After this, a P-TEOS film 17 is formed on the substrate surface as shown in Fig. 1. Depending upon the situation, multiple levels of interconnect are then formed by repeating steps similar to those described above, after the contact hole is formed. In the present embodiment, the interconnect structure was built up to the second level by forming an interconnect 18. Finally, the entire surface of the substrate is coated by CVD with a phosphorus-laced silicon oxide film 19 and then with an insulating film containing nitrogen to obtain a passivation film 20. After this, a semiconductor device having a cross-sectional structure shown in Fig. 1 is formed by etching the passivation film 20. In the present embodiment, a CMOS comprised of an n-type MOS and a p-type MOS having a gate length of 0.5 μm and a gate width of 15 μm was obtained.

[0065] Next, the lifetime of hot carriers was determined with respect to MOS transistors manufactured by the method such as the one of the present embodiment. The resistivity of the nitrogen-laced insulating films 12 and 14 to water permeation can be evaluated by determining the lifetime of hot carriers. In other words, if the lifetime of hot carriers (electrons and holes) of

an MOS transistor during operation is long, then the water-permeation resistance of each of these insulating films 12 and 14 can be evaluated as good. On the other hand, if the lifetime of hot carriers is short, then the water-permeation resistance can be rated as poor.

[0066] In the determination, the lifetime of hot carriers was obtained by calculation using the mutual conductance G_m (= dI_d / dV_g*) of the MOS transistor. Firstly, changes in the drain electric current I_d with respect to changes in the gate voltage V_g are measured while a drain voltage V_d of 0.1 (V) is applied. From the graph obtained by plotting the profile of changes in the drain current against changes in the gate voltage, the maximum value G_{m0} for the mutual conductance G_m is obtained. The DC stress condition that would yield the maximum substrate current is applied on the transistor for a predetermined period of time, for example, when the drain voltage V_d is 5.5 (V), DC stress produced by a gate voltage V_g of 1.75 (V) is applied. Then, changes in the drain current I_d with respect to changes in the gate voltage V_g are again measured while a drain voltage V_d of 0.1 (V) is applied. The maximum value G_{mT} for the mutual conductance G_m is then obtained from the results of these determinations. Then, the percentage decline in the maximum value of the mutual conductance G_m is obtained from the following equation.

[0067]

$$\{(G_{m0} - G_{mT}) / G_{m0}\} \times 100\ (\%)$$

The above determination to obtain the percentage was repeated by varying the duration of the DC stress applied, in order to obtain the percentage decline in the maximum value of mutual conductance as a function of variation in the duration of stress applied. The graph shown in Fig. 6 was obtained in this manner, under the following DC stress condition: a gate voltage V_g = 1.75 (V) and a drain voltage V_d = 5.5 (V). The abscissa of the graph represents the stress time (sec.), whereas percentage (%) decline in the maximum value of the mutual conductance G_m is represented on the ordinate.

[0068] Moreover, these determinations were carried out not only with the MOS transistor obtained by the foregoing embodiment but also with a variety of comparative transistors in a similar manner. Of the transistors used for the comparison, device 1 is a semiconductor device that lacks both of the insulating films 12 and 14, both of which were doped with nitrogen during the manufacturing process in the foregoing embodiment. In other words, this device was not exposed to gas plasma containing nitrogen after the patterning of the interconnect 11, nor was the surface of its P-TEOS film 13 exposed to gas plasma containing nitrogen. In the case of comparison device 2, although its nitrogen-laced insulating film 14 was formed in a similar manner to that of the embodiment, its nitrogen-laced insulating film 12 was formed in a different manner. In other words, in comparison device 1, the film was formed, not after the interconnect 11 had been patterned, but after a contact hole had been formed in the BPSG film 10, but before BHF treatment to form a metal film, by exposing the substrate surface to gas plasma containing nitrogen. Moreover, in the case of comparison device 3, the nitrogen-laced insulating film 12

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* Translator's note: The subscript in the original illegible; might be "V_q".

was formed in between the interconnect 11, as is the case with the transistor of the embodiment, but the nitrogen-laced insulating film 14 was not formed, because the surface of the p-TEOS film 13 was not exposed to plasma. In other words, the comparison device 3 is a variant of the embodiment. Since comparison device 4 was formed by the foregoing embodiment, it was provided with both the nitrogen-laced insulating film 12 and the insulating film 14. In other words, it was exposed to a plasma after the metal interconnect had been formed, and the surface of P-TEOS film 13 was also exposed to plasma.

[0069] In the graph, curve A plotted with open circles (○) was obtained for comparison device 1, whereas curve B plotted with open triangles (△) was obtained for comparison device 2, curve C plotted with solid circles (●) for comparison device 3, and curve D plotted with open squares (□) for comparison device 4.

[0070] Table 1 given below shows the lifetime of hot carriers obtained in the following manner: the duration of DC stress applied needed to obtain a 10% decline in the maximum value of mutual conductance G_m was obtained from the graph, and the duration of DC stress applied thus obtained was taken as the lifetime of hot carriers.

[0071]

Table 1.

	Metal Interconnect Exposed to Plasma	P-TEOS Film Exposed to Plasma	Hot-Carrier Lifetime
Comparison Device 1	No	No	5,800 sec.
Comparison Device 2	Treated with nitrogen plasma after contact hole formed	Yes	8,200 sec.
Comparison Device 3	Yes	No	62,200 sec.
Comparison Device 4	Yes	Yes	135,000 sec.

[0072] As indicated in the table, the lifetime of hot carriers is 5,800 seconds for the comparison device 1, whose metal interconnect 11 and P-TEOS film 13 were not exposed to plasma. The lifetime of hot carriers is 8,200 seconds for the comparison device 2, which was treated with plasma after a contact hole had been formed. On the other hand, the hot-carrier lifetime is longer, 62,200 seconds, for the comparison device 3, which is a variant of the present embodiment and has a nitrogen-laced insulating film 12, and this is about ten times longer than the lifetime of the comparison device 1 or 2. In the case of the comparison device 4 of the

present embodiment, because it is provided with an insulating film 14, in addition to the nitrogen-laced insulating film 12, its hot-carrier lifetime is even longer at 135,000 seconds, which is about twice that of the comparison device 3.

[0073] The short hot-carrier lifetime of the comparison device 1, which was not exposed to a nitriding plasma, is caused by the fact that the moisture contained in the SOG film 16, O_3-TEOS film 15 and P-TEOS film 13 is diffused into the gate oxide film 5 of the MOS transistor to generate traps there. On the other hand, in the case of the comparison device 2, which was exposed to plasma after the contact hole had been formed, the hot-carrier lifetime is 8,200 seconds, which is longer than that of the comparison device 1. However, this is not a conspicuous effect. This is because, even though a nitrogen-laced insulating film is formed on the surface of the BPSG film 10 by exposure to plasma, it is stripped thinner by the subsequent BHF treatment and etching carried out to pattern the interconnect 11. As a result, even though the diffusion of the moisture contained in the SOG film 16 and O_3-TEOS film 15 is blocked by the nitrogen-laced insulating film 14, the moisture contained in the P-TEOS film 13 is diffused into the gate oxide film 5 of the MOS transistor during heat treatment to form traps there, because the nitrogen-laced insulating film on the BPSG film 10 has become thinner, as described earlier.

[0074] On the other hand, a longer hot-carrier lifetime is obtained for the comparison device 3, which is a variant of the present embodiment. This is because, even through the nitrogen-laced insulating film 14 is lacking, a nitrogen-laced insulating film 12 is formed in the layer underneath. In other words, the diffusion of the moisture contained in the SOG film 16, O_3-TEOS film 15 and P-TEOS film 13 is mostly blocked by the nitrogen-laced insulating film 12, thus preventing the diffusion of moisture into the gate oxide film 5 of the MOS transistor. As a result, no traps are formed in the gate oxide film, thereby greatly reducing the likelihood of hot carriers being captured by traps. In the case of the comparison device 4 of the present embodiment, moreover, the lifetime of hot carriers is even longer. This is because it is provided with the nitrogen-laced insulating film 14, in addition to the nitrogen-laced insulating film 12. Therefore, the diffusion of moisture is blocked by two insulating films 12 and 14. In this manner, the comparison devices 3 and 4 according to the present invention can prevent the formation of traps caused by the diffusion of moisture into the gate oxide film 5, thereby preventing the accelerated degradation of the lifetime of hot carriers. As a result, the present invention makes it possible to provide a semiconductor device that can sufficiently withstand practical use.

[0075] The foregoing embodiment was described using an n-type MOS transistor having an LDD structure. However, the present invention should not be limited to what was described above, but it may also be applied to semiconductor devices having p-type MOS transistors or semiconductor devices having MOS transistors with a single-drain structure, and similar effects are also obtained in these instances. Moreover, in the description of the foregoing embodiment, the BPSG film 10 was used as the insulating film under the metal interconnect 11 and the P-TEOS film 13 as the insulating film over the metal interconnect 11, but these insulating films should not be limited to these films. For example, silicon oxide films that have been formed in a

plasma under reduced or normal pressure or insulating films containing nitrogen (a low concentration of nitrogen at a level to allow the passage of moisture), nitride films, as well as other insulating films and SOG films made from organic silane, may also be used in place of the BPSG film 10 or P-TEOS film 13. Exposing the surface of these insulating films to plasma containing nitrogen also results in the formation of highly water-permeation resistant insulating films containing nitrogen on the surface, thus effects that are similar to those obtained by the foregoing embodiments are obtained.

[0076] A semiconductor device and a method of manufacturing the same according to a second embodiment of the present invention as applied to a CMOS transistor will be described hereinafter with reference to accompanying diagrams, Fig. 7 to Fig. 9. Even though a CMOS transistor is constructed by combining an n-type MOS and a p-type MOS, only the n-type MOS is shown in these diagrams. Moreover, parts that are the same as or correspond to those of Fig. 1 are designated by the same reference numerals.

[0077] Firstly, a p-well 2, a channel stopper 3 and a silicon oxide film 4 for isolating the element are formed on a p-type silicon substrate 1, as shown in Fig. 7. Then, a gate oxide film 5, a polysilicon film 6 and a tungsten silicide film 7 are stacked to form a gate electrode. The first ion implantation is then carried out using the gate electrode as a mask, to be followed by the second ion implantation using the gate electrode and side walls 8 as a mask, to form a source region and a drain region, not shown in the diagram, having an LDD structure. A silicon oxide film 9 is then formed on the entire surface of the substrate, and a BPSG film 10, which contains boron and phosphorus, is formed on the silicon oxide film 9. The surface of the BPSG film 10 is made flat by heat treatment. Steps up to this stage are carried out in the same manner as those of the first embodiment.

[0078] Next, a P-SiO film 21 is formed on top of the BPSG film 10. The P-SiO film 21 is formed in a plasma from SiH_4, N_2O and N_2 using the gas flow ratio as follows: the gas flow rate of SiH_4 with respect to the sum of that of N_2O and N_2 (= SiH_4 / (N_2O + N_2)) is in the range of 0.055 to 0.086. Here, a number of P-SiO films 21 were formed using various flow ratios, as follows: SiH_4 / (N_2O + N_2) = 0.048, 0.051, 0.055, 0.063, 0.074, 0.086 and 0.1. They are to be used in the comparative determination of the hot-carrier lifetime described later.

[0079] After this, the P-SiO film 21, the BPSG film 10 and the silicon oxide film 9 were selectively etched to create a contact hole, which is not shown in the diagram, reaching to the source and drain regions of the MOS transistor. After the substrate surface is washed by BHF treatment, a metal interconnect layer composed of an Al alloy is formed by sputtering. A desired metal interconnect 11 is then formed by patterning the metal interconnect layer, as shown in Fig. 8. A P-TEOS film 13 is then formed to envelope the metal interconnect 11. An O_3-TEOS film 15 and an SOG film 16 are then formed on the P-TEOS film 13. The SOG film 16 is then etched to make the substrate surface flat. After this, another P-TEOS film 17 is formed on the flattened SOG film 16.

[0080] After the contact hole is opened, a second layer of metal interconnect 18 is formed as shown in Fig. 9. Depending upon the situation, all of the steps starting from that for forming the first layer of metal interconnects 11 up to that for forming the second layer of the metal interconnect 18 are repeated to form multiple levels of interconnect. In the present embodiment, the interconnect was built up to the second level by forming the metal interconnect 18. A silicon oxide film 19 containing phosphorus is then formed on the metal interconnects 18 by CVD. Finally, a silicon nitride film is formed on the silicon oxide film 19 by CVD, to obtain a passivation film 20. An electrode is then formed by etching the passivation film 20, to obtain a finished semiconductor device.

[0081] With a semiconductor device such as the one obtained by the second embodiment, moisture contained in the SOG film 16 and the O_3-TEOS film 15 tries to diffuse into the MOS transistor section, but bonds such as Si-H, Si-NH and Si-N present in the P-SiO film 21 react with the diffused moisture to produce silicon oxide. Therefore, the diffusion of moisture contained in the interlayer insulating film into the transistor section is effectively prevented in the semiconductor device of the second embodiment. This can be confirmed by the experiment described below.

[0082] In this experiment, a semiconductor substrate having a P-SiO film 21 on its surface according to the present embodiment was immersed in heavy water (D_2O) maintained at 80°C for 24 hours. The concentration of each constituent element was determined before and after the immersion in heavy water by Fourier transform infrared spectroscopy (FTIR). Fig. 10 is a graph showing the results of the analysis carried out on the P-SiO film 21 by Fourier transform infrared spectroscopy. Here, the wave number (cm^{-1}) of the light measured is given on the abscissa, while the absorbance is given on the ordinate. Moreover, spectrum A is the result of the analysis of the P-SiO film 21 prior to the immersion in heavy water, whereas spectrum B is the result of the analysis of the P-SiO film 21 carried out after the semiconductor substrate had been immersed in heavy water.

[0083] As shown in the graph, the absorbance peak for each of Si-O, Si-H, Si-NH and Si-N bonds is observed for both spectra A and B. In the case of spectrum B, which was measured after the substrate was allowed to stand in heavy water at 80°C for 24 hours, the peak strength for each of the Si-H, Si-NH and Si-N bonds of the P-SiO film 21 is all weaker than that of the spectrum A. Moreover, two absorbance peaks are found for Si-O bonds at 450 cm^{-1} and at 1,080 cm^{-1}. The strength of the absorbance peak of Si-O bonds near the wave number of 1,080 cm^{-1} seems either the same or somewhat less than that of spectrum A, but this is unclear because it is superimposed with the peak of Si-NH bonds. The strength of the absorbance peak of Si-O bonds near the wave number 450 cm^{-1} is showing an increase in spectrum B obtained after immersion in heavy water. In other words, while Si-H, Si-NH, and Si-N bonds have decreased, Si-O bonds have increased. Therefore, it is conceivable that the diffused water is reacting with the Si-H, Si-NH, and Si-N bonds in the P-SiO film 21 according to the reaction equations given in (1) to (3) below, i.e., reactions that will yield a silicon oxide film are taking place there.

[0084] The chemical reaction between Si-H bonds and water takes place according to the following equation (1).

[0085]

$$2\ \text{Si-H} + H_2O \rightarrow \text{O-Si-O} + 2\ H_2 \uparrow \qquad \ldots (1)$$

The chemical reaction between Si-NH bonds and water takes place according to the following equation (2).

[0086]

$$\text{Si-NH} + 2\ H_2O \rightarrow \text{O-Si-O} + NH_3 \uparrow + H_2 \uparrow \qquad \ldots (2)$$

The chemical reaction between Si-N bonds and water takes place according to the following equation (3).

[0087]

$$2\ \text{Si-N} + 4\ H_2O \rightarrow 2\ \text{O-Si-O} + 2\ NH_3 \uparrow + H_2 \uparrow \qquad \ldots (3)$$

The Si-NH bonds produced during the reaction process further reacts with water according to the equation (2).

[0088] The graph of Fig. 11 shows the results of the evaluation of water permeability, with respect to heavy water, of various P-SiO films, which were formed using various flow ratios of gases introduced and expressed by $SiH_4 / (N_2O + N_2)$. As was the case with the FTIR determination, the evaluation was carried out by analyzing the quantity of deuterium D contained in the P-SiO film 21 by the secondary ion mass spectroscopy (SIMS) after the semiconductor substrate 8 with the P-SiO film 21 formed on it had been immersed in heavy water at 80°C for 24 hours. The depth from the film surface (μm) of the P-SiO film 21 is given on the abscissa, while the deuterium (D) concentration (atoms/cm^3) of the film at various depths is given on the ordinate. Moreover, the spectra A, B, C are the results of determination obtained for the $SiH_4 / (N_2O + N_2)$ flow ratio of 0.0476, 0.0616 and 0.0739, respectively.

[0089] As the graph shows, because the concentration of heavy water decreases as the flow rate ratio of $SiH_4 / (N_2O + N_2)$ increases, it is found that the resistance against water permeability is improved at the flow ratio values of 0.0616 and 0.0739, which are within the range of the flow ratio of the present embodiment. It is also demonstrated that the decrease in the concentration of deuterium becomes vertical* at the flow ratio of 0.0616 in spectra B. This is because at a flow ratio higher than this, the concentration of hydrogen will either increase or the concentration of nitrogen (Si-N and Si-NH) will reach saturation. The reason for this increase in the concentration of nitrogen to the point of saturation even though the increase in the flow ratio would cause a reduction in the percentage of N_2O is this: when unbonded Si, which has

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* Translator's note: The word in the original is "saturated".

increased with the increase in the flow ratio, forms a film in plasma, the nitrogen used as a carrier gas is ionized and bonds with Si. Therefore, if the SiH_4 / (N_2O + N_2) flow ratio were to become too large, there would not be enough nitrogen, because the nitrogen concentration would become saturated, and this would result in a decline in the resistance of the P-SiO film 21 against water permeation. Moreover, if the concentration of hydrogen becomes excessive as a result of an increase in the flow ratio, this would have the opposite effect because hydrogen would drift away. As a result, hydrogen that has drifted away would be diffused into the gate, thereby compromising hot-carrier tolerance.

[0090] In other words, the concentrations of both hydrogen and nitrogen in the P-SiO film 21 needs to be within certain ranges. As will be described later, a metal-oxide silicon field-effect transistor (MOSFET) having a P-SiO film 21, whose hydrogen and nitrogen concentrations have been limited to the range of 1×10^{21} to 5×10^{22} atoms/cm^3 for hydrogen and 1×10^{21} to 2×10^{22} atoms/cm^3 for nitrogen, as the interlayer film provides a semiconductor device without compromising its hot-carrier tolerance. The P-SiO film 21 having such hydrogen and nitrogen concentrations, as will be described later, is obtained by forming a silicon oxide film by plasma-enhanced CVD with a flow ratio of SiH_4 / (N_2O + N_2) = 0.055 to 0.086.

[0091] Next, the lifetime of hot carriers was determined using MOS semiconductor devices manufactured by the method according to the present embodiment. The semiconductor devices used for this determination were those having the P-SiO film 21, which were formed using the values described earlier for the SiH_4 / (N_2O + N_2) flow ratio. Moreover, as a comparison, the same determination was carried out with the following two semiconductor devices. More particularly, the determination was carried out with the semiconductor device of the present embodiment shown in Fig. 9, having a two-level interconnect structure but not provided with the P-SiO film 21. The determination was also carried out with a semiconductor device having a single-level interconnect structure with a phosphorus-doped silicon film 22 formed by CVD directly on the P-TEOS film 13, which is on the first metal interconnect 11, without forming the second interlayer film after the first metal interconnect 11 is formed, as shown in Fig. 12. Incidentally, with Fig. 12, members that are the same as or correspond to those of Fig. 9 are designated by the same reference numerals and explanation thereof will be omitted. All semiconductor devices used for the experiment were n-type MOS semiconductor devices having a gate length of 0.5 μm and a gate width of 10 μm.

[0092] The water permeability of the P-SiO film 21 can be evaluated by determining the lifetime of hot carriers. In other words, if the lifetime of hot carriers is long while the n-type MOS semiconductor device is in operation, then the resistance of the P-SiO film 21 against water permeation is evaluated as good. On the other hand, if the hot-carrier lifetime is short, the film is evaluated as having a poor resistance to water permeation. In the determination, the lifetime of hot carriers was calculated from the mutual conductance G_m (= dI_d / dV_g) of the n-type MOS semiconductor device in the following manner, as was the case with the first embodiment. Firstly, changes in the drain electric current I_d with respect to changes in the gate voltage V_g are measured while a drain voltage V_d of 0.1 (V) is applied. From the graph obtained by plotting the profile of changes in the drain current against changes in the gate voltage, the

maximum value G_{m0} for the mutual conductance G_m is obtained. The DC stress condition that would yield the maximum substrate current is applied on the semiconductor device for a predetermined period of time. Then, changes in the drain current I_d with respect to changes in the gate voltage V_g are again measured while a drain voltage V_d of 0.1 (V) is applied. The maximum value G_{mT} for the mutual conductance G_m is then obtained from the results of these determinations. Then, the percentage decline in the maximum value of the mutual conductance G_m is obtained from the following equation.

[0093]

$$\{(G_{m0} - G_{mT}) / G_{m0}\} \times 100\ (\%)$$

The above determination to obtain the percentage were repeated by varying the duration of the DC stress applied, in order to obtain the percentage decline in the maximum value of mutual conductance as a function of changes in the duration of stress applied. The graph of Fig. 13 shows the typical time dependence of the percentage decline of mutual conductance. The stress time (in sec.) is plotted on the abscissa of the graph, whereas percentage (%) decline in the maximum value of the mutual conductance G_m is plotted on the ordinate. The line plotted with triangles (△) was obtained with the semiconductor device of the present embodiment wherein the P-SiO film 21 was formed using a flow ratio of $SiH_4 / (N_2O + N_2) = 0.055$, whereas the line plotted with squares (□) was obtained with the semiconductor device of the present embodiment, wherein the P-SiO film 21 was formed using a flow ratio of $SiH_4 / (N_2O + N_2) = 0.0739$. Moreover the line plotted with circles (○) was obtained with the semiconductor device, wherein the P-SiO film 21 was formed using a flow ratio of $SiH_4 / (N_2O + N_2) = 0.0476$ but not according to the present embodiment, whereas the line plotted with x's was obtained with the aforementioned semiconductor device having a two-level metal interconnect structure. The line plotted with solid diamonds (◆) was obtained with the semiconductor device having a single-level metal interconnect structure.

[0094] With the graph of Fig. 13, the time needed to obtain a 10% decline in the maximum value of mutual conductance G_m, i.e., the time required to obtain $\{(G_{m0} - G_{mT}) / G_{m0}\} \times 100 = 10\%$, was defined as the lifetime of hot carriers. The dependence of the lifetime of hot carriers on the $SiH_4 / (N_2O + N_2)$ flow ratio is shown in Fig. 14. Here, the abscissa represents the $SiH_4 / (N_2O + N_2)$ flow ratio, whereas the ordinate represents the lifetime of hot carriers (in sec.). Since the semiconductor device having a single-level metal interconnect structure and the one having a two-level interconnect structure are not provided with the P-SiO film, they do not have this dependence on the flow ratio. Because the semiconductor device having a single-level metal interconnect structure does not have a moisture-laced interlayer insulating film, the lifetime of hot carriers is long, since it is not affected by the diffusion of moisture, as demonstrated by the straight line A in the graph. Moreover, because the semiconductor device having a two-level metal interconnect structure is not provided with the P-SiO film, the moisture present in the interlayer insulating film is directly diffused into the gate section of the MOSFET. As a result, the lifetime of hot carriers of the device is short, as demonstrated by the straight line B in the graph.

[0095] In the case of the semiconductor device not according to the present embodiment, wherein the P-SiO film was formed using the flow ratio of 0.048, the lifetime of hot carriers is the same as that of the semiconductor device having a two-level metal interconnect structure but no P-SiO film, as demonstrated by the graph, so this shows no effect in preventing the diffusion of water. However, when the P-SiO film 21 was formed using the SiH_4 / (N_2O + N_2) flow ratio within the range of 0.055 to 0.086 according to the present embodiment, the lifetime of hot carriers was long, the same as that obtained for the semiconductor device having a single-level metal interconnect structure. Therefore, the diffusion of water was completely prevented.

[0096] Moreover, as shown in Fig. 15, the P-SiO film 21 of the present embodiment having a hydrogen concentration of 1×10^{21} to 5×10^{22} atoms/cm^3 and a nitrogen concentration of 1×10^{21} to 2×10^{22} atoms/cm^3 can be obtained by forming a silicon oxide film by plasma-enhanced CVD using a flow ratio within the range of SiH_4 / (N_2O + N_2) = 0.055 to 0.086. In Fig. 15, the abscissa represents the flow ratio, while the ordinate represents the concentration of hydrogen or nitrogen (atoms/cm^3). Moreover, the plot indicated by circles (○) was obtained for nitrogen, whereas the plot indicated by squares (□) was obtained for hydrogen. When the P-SiO film 21, whose hydrogen and nitrogen concentrations are limited to this range, is used for a transistor having a multi-layer film structure, the diffusion of moisture contained in the interlayer insulating film, i.e., the SOG film 16 or the O_3-TEOS film 15, into the gate section can be completely prevented, thus providing a semiconductor device whose hot-carrier tolerance is not compromised.

[0097] Incidentally, the foregoing embodiment was described with reference to instances in which the P-SiO film 21, which prevents the diffusion of moisture, was formed on the BPSG film 10. However, the P-SiO film 21 may be placed anywhere between the MOSFET gate section and the interlayer insulating film, which contains water, and this would yield effects similar to those obtained for the foregoing embodiment.

[0098] Moreover, the foregoing embodiment was described with reference to an n-type semiconductor device having an LDD structure. However, it should not be limited to this, for p-type semiconductor devices or those having a single-drain structure may also be used. Moreover, effects similar to those obtained for the foregoing embodiment would be obtained by the use of semiconductor devices using chemical-compound semiconductors such as gallium arsenide (GaAs).

[0099] A semiconductor device and the method of manufacturing the same according to a third preferred embodiment of the present invention will be described hereinafter.

[0100] Fig. 16 is a schematic diagram of a plasma-enhanced CVD apparatus for forming the P-SiO film used in the present embodiment. This is a commonly used parallel-plane type plasma-enhanced CVD apparatus, with conductive plates 33 and 34, which can be used to hold a semiconductor substrate 32, located inside the reactor 31. A plasma excitation power source 35 is connected to the conductive plates 33 and 34. Moreover, a heater 36 is installed under the

conductive plate 34. Gas inlet openings for SiH_4, N_2O, O_2, N_2 and the like are also located in the reactor 31. Although this is not shown in the diagram, since the reactor 31 is connected to a vacuum exhaust system, its interior can be maintained at high vacuum.

[0101] As for the method of forming the P-SiO film, the temperature of the substrate is raised to 350°C by heating the interior of the reactor 31 to 350°C, and after the pressure is reduced to 0.35 torr, SiH_4 is supplied at a rate that is within the range of 45 to 500 sccm, e.g., at 100 sccm, and N_2O at a rate that is within the range of 1,000 to 2,000 sccm, e.g., at 1,850 sccm. After these gas flow rates have stabilized, the plasma excitation power source 35 is applied using an RF excitation wave number of 50 KHz and an RF power of 500 W for a prescribed period of time, to form a P-SiO film of 0.3 μm.

[0102] The hydrogen content supplied by Si-H bonds as a function of the film-formation rate and of the Si/O ratio for P-SiO films are shown in Fig. 17 and Fig. 18. Fig. 17, is a graph showing the relationship between the H content (atoms/cm^3), plotted on the abscissa, and the film-formation rate (angstroms/min), on the ordinate. Fig. 18 is a graph showing the relationship between the H content (atoms/cm^3), given on the abscissa, and the O/Si ratio, given on the ordinate. With the P-SiO film, which is important to the present embodiment, the H content supplied by Si-H bonds present in the film can be varied substantially by changing the flow ratio of chiefly silane gas and dinitrogen oxide gas. In the graph, the H content supplied by Si-H bonds present in the P-SiO film was determined by FTIR.

[0103] The results of the determination of the film-formation rate and the Si/O ratio presented in the graph demonstrate that, when the hydrogen content supplied by Si-H bonds exceeded 5×10^{22} /cm^3, the film was silicon-rich (close to amorphous silicon). Consequently, a P-SiO film with a hydrogen content of 5×10^{22} /cm^3 or less must be used.

[0104] Moreover, the diffusion of deuterium into the P-SiO film was determined in order to study the diffusion of hydrogen in the P-SiO film by analyzing the film in the depth direction using secondary ion mass spectroscopy (SIMS). The results thus obtained are shown in Fig. 19. The results demonstrated that when the H content supplied by Si-H bonds in the P-SiO film exceeded 5×10^{20} /cm^3, the diffusion of deuterium (moisture) could be substantially suppressed by the P-SiO film, whereas the film's ability to suppress the diffusion of moisture was highly compromised when the H content was 5×10^{20} /cm^3 or less.

[0105] In other words, in order to eliminate the disadvantages of the conventional interlayer insulating films, the ability of plasma oxide films made from SiH_4 to block mobile ions and the like was investigated thoroughly. As a result, it was found that when the hydrogen content supplied by Si-H bonds in the oxide film is 5×10^{20} /cm^3 or less, mobile ions and the like are not captured to a sufficient degree, resulting in the degradation of the transistor's properties. Moreover, if the hydrogen content supplied by Si-H bonds in the oxide film exceeds 5×10^{22} /cm^3, the film-formation rate of the film being formed becomes extremely low, so that it cannot be put to practical use. Furthermore, in this case, the film formed is more like amorphous

silicon than an oxide film, so that it would not be possible to process the film further in subsequent steps such as the one for forming via holes.

[0106] Consequently, when a semiconductor is made using a film having a high mobile-ion content by providing it with an insulating film having an oxide-film structure with its plasma oxide film's hydrogen content supplied by Si-H bonds at 5×10^{20} /cm^3 or more but 5×10^{22} /cm^3 or less, the plasma oxide having such a prescribed hydrogen content suppresses the diffusion of mobile ions and the like from the film that has high content of these ions and the like. Thus, a semiconductor device with an excellent durability against the degradation of the transistor properties is provided.

[0107] Although the mechanism whereby Si-H in the plasma oxide film blocks the diffusion of mobile ions and the like is unknown, the guess is that, in the case of water, for example, water is blocked by reactions such as $2\ \text{Si-H} + \text{H}_2\text{O} \rightarrow \text{Si-O-Si} + 2\ \text{H}_2 \uparrow$. Incidentally, besides increasing or decreasing the SiH_4 quantity, for example, methods such as the one in which H_2, NH_3 and the like are added to the reaction gas are effective as more specific means of controlling the hydrogen content of the plasma oxide film,.

[0108] Next, one example of a method for flattening the interlayer insulating film using the P-SiO film will be described. Fig. 20 is a cross-sectional view of a semiconductor device having an aluminum multilevel interconnect structure. A silicon oxide film 42 is formed by a vapor deposition method or by doping with phosphorus or boron on a semiconductor substrate 41, wherein an MOS integrated circuit has been formed on its surface by a commonly used method. After a contact hole, not shown in the diagram, is formed on the desired location of the silicon oxide film 42, a first interconnect 43 is formed from materials such as aluminum, to be followed by patterning by a commonly used method. A P-SiO film 44 is then formed by means of the plasma-enhanced CVD apparatus shown in Fig. 16 in order to obtain an interlayer insulating film. Then, after an SOG film 45 is applied by means of a spin coater, heat treatment is carried out at 400°C. Furthermore, these films are etch-backed to form a 0.6-μm thick P-SiO film 46 by the same method as that used for the P-SiO film 44. After through holes are formed at the desired locations of the interlayer insulating film, a second interconnect 47 is formed from materials such as aluminum. In this manner, a finished semiconductor device having a multilevel interconnect structure is obtained. Although the SOG film was used as the interlayer film in this flattening process, it goes without saying that other methods (a chemical mechanical polishing method, for example) may also be used.

[0109] The relationship of the H content supplied by Si-H bonds in the P-SiO films 44 and 46 with the reliability of the transistor fabricated according to this method was tested using the lifetime of hot carriers. The results thus obtained are shown in the graph of Fig. 21. The lifetime of hot carriers was determined by calculating it from the mutual conductance G_m of the n-type MOS semiconductor device in the following manner, as was the case in the foregoing first and second embodiments. In other words, as described earlier, the maximum value G_{m0} for the mutual conductance G_m is obtained. Then, the DC stress condition that would yield the maximum substrate current is applied on the semiconductor device for a predetermined period of

time. The maximum value G_{mT} for the mutual conductance G_m is then obtained, and the percentage decline in the maximum value of the mutual conductance G_m is obtained from the following equation.

[0110]

$$\{(G_{m0} - G_{mT}) / G_{m0}\} \times 100\ (\%)$$

The above determinations to obtain the percentage were repeated by varying the duration of the DC stress applied, in order to obtain the percentage decline in the maximum value of mutual conductance as a function of changes in the duration of stress applied. The graph of Fig. 21 shows the typical time dependence of the percentage decline of mutual conductance. The abscissa of the graph represents the stress duration (in sec.), whereas percentage (%) decline in the mutual conductance is represented on the ordinate. The line plotted with open circles (○) was obtained when the H concentration supplied by Si-H bonds was 3.6×10^{19}, the line plotted with solid circles (●) when the H concentration supplied by Si-H bonds was 3.6×10^{20}, the line plotted with solid squares (■) when the H concentration supplied by Si-H bonds was 5.0×10^{20}, and whereas the line plotted with open squares (□) was obtained when the H concentration supplied by Si-H bonds was 1.2×10^{21}.

[0111] The results of this experiment also showed that when the H concentration supplied by Si-H bonds was 5×10^{20} /cm^3 or more, the lifetime of hot carriers was about 10 times longer than that obtained when the H concentration supplied by Si-H bonds was 5×10^{20} /cm^3 or less. As well, they demonstrated that the distribution of mobile ions was suppressed by the P-SiO films 44 and 46.

[0112] A fourth preferred embodiment of the present invention as applied to a method of manufacturing a CMOS will be described now. Fig. 22 to Fig. 27 are cross-sectional views illustrating a manufacturing method according to the present embodiment. Although a CMOS is constituted by combining an n-type MOS with a p-type MOS, only the n-type MOS is shown in these diagrams.

[0113] Firstly, as shown in Fig. 22, a silicon oxide film having a thickness of about 500 angstroms is formed on the surface of a p-type silicon substrate 51 by oxidizing the surface. Then, boron ions are implanted, through the silicon oxide film, into the region where an n-type MOS is to be formed using a dose of around 1.2×10^{13} /cm^2, to form a p-well 52. The region where a p-type MOS is to be formed is implanted with phosphorus ions using a dose of around 1.35×10^{13} /cm^2 to form an n-well, not shown in the diagram. Heat treatment is then carried out to diffuse the implanted boron and phosphorus in order to enlarge each of the well regions. Then, after the silicon oxide film on the substrate surface is etched, a pad oxide film is formed on it. A silicon nitride film is then formed on the pad oxide film by CVD. The silicon nitride film in the inactive region where the transistor is not to be formed is removed selectively, to leave intact the silicon nitride film in the active region, where the transistor is to be formed. Channel stopper ions are selectively implanted into the inactive region of the p-type silicon substrate 51, to form a channel stopper 53. A silicon oxide film 54, which has a thickness of 6,000 angstroms

and whose purpose is to isolate the element, is formed in the inactive region by thermal oxidation, thus providing insulation between elements.

[0114] Boron fluoride ions, for the purpose of regulating the threshold value, are then implanted into the active region at a dose of around 2.7×10^{12} /cm^2. Then, after the pad oxide film is removed by wet-etching, a gate oxide film 55 consisting of a silicon oxide film is formed on the exposed well regions, and a polysilicon film 56 is formed on the gate oxide film 55 by CVD. The resistance of the polysilicon film 56 is then reduced by doping it with phosphorus. A tungsten silicide film 57 is then formed by sputtering. After this, the tungsten silicide film 57, the polysilicon film 56 and the gate oxide film 55 are selectively etched to form a gate electrode.

[0115] Next, phosphorus ions are implanted into the entire surface of the p-well 52 using a dose of around 2.0×10^{13} /cm^2, while boron fluoride ions are implanted into the entire surface of the n-well using a dose of 5.0×10^{12} /cm^2. As a result of these ion implantations, a low-concentration region 58 is formed for the source and the drain. Next, after a silicon oxide film is formed on the substrate surface by CVD, this silicon oxide film is etched back, to form sidewalls 59 on all sides of the gate electrode. After this, the substrate surface is usually washed with a mixed solution of H_2SO_4 and H_2O. For a comparison, an unwashed n-type MOS was also fabricated. The entire surface of the semiconductor substrate was exposed to fluorine plasma or gas plasma containing fluorine from the angle indicated by the arrows in Fig. 22. This exposure to plasma is carried out using a gas mixture of nitrogen containing 2% NF_3 at a temperature of 400°C. The exposure to fluorine plasma or gas plasma containing fluorine carried out in the subsequent steps of the present embodiment is also performed under the same conditions. Next, arsenic ions are implanted into the source and drain regions on the side of the p-well 52 using a dose of around 3×10^{15} /cm^2. On the other hand, boron fluoride ions are implanted into the source and drain regions on the side of the n-well, not shown in the diagram, using a dose of around 1.5×10^{15} /cm^2 to form a high-concentration region 60 for the source and the drain. Thus, the source and drain regions having an LDD (lightly doped drain) structure are formed.

[0116] Next, after a silicon oxide film 61 is formed at a low temperature to cover the entire surface of the substrate, the latter is exposed to fluorine plasma or gas plasma containing fluorine from the direction indicated by the arrows in Fig. 23. As a result, a silicon oxide film (BPSG film) 62 containing boron and phosphorus is formed on top of the silicon oxide film 61 and covering the entire surface of the substrate, as shown in Fig. 24. After this, the surface of the BPSG film 62 is flattened by heat treatment at 900°C for 15 minutes. The BPSG film 62 and the silicon oxide film 61 below it are selectively etched to form a contact hole penetrating through to the drain and source regions of the transistor, but not shown in the diagram. Then, after the substrate surface is washed by BHF treatment, an aluminum (Al) alloy film is formed on the entire surface of the substrate by sputtering. After this, a resist is applied on the Al alloy film and then patterned using a photolithography technique. The Al alloy film is then etched using the resist as a mask to obtain an interconnect 63 of a desired shape. The resist 64 is then stripped away with an organic washing solution, and the entire surface of the semiconductor substrate is exposed to fluorine plasma or gas plasma containing fluorine, as shown in Fig. 25.

[0117] Then, a P-TEOS film 65 is formed on the substrate surface, as shown in Fig. 26. After an O_3-TEOS film 66 and an SOG film 67 are formed in sequence on the P-TEOS film 65, the SOG film 67 is etched to make the substrate surface flat. Another P-TEOS film 68 is then formed on the substrate surface. Then, after a contact hole is formed, an Al alloy film is formed on the entire surface of the substrate, and a resist is applied on the Al alloy film and patterned by photolithography. The Al alloy film is then etched using the resist as a mask, to obtain a desired metal interconnect 69, as shown in Fig. 27. After the resist is stripped away with an organic washing solution, the entire surface of the semiconductor substrate is exposed to fluorine plasma or gas plasma containing fluorine. Depending on the situation, the same steps as those described above are repeated to form multiple levels of interconnect. With the present embodiment, the multilevel interconnect structure was built up to the second level by forming the interconnect 69. Finally, a phosphorus-doped silicon oxide film 70 is formed by CVD. Furthermore, a passivation film 71 is formed by coating the entire surface of the substrate with a silicon nitride film and then etched to complete the fabrication of a semiconductor device having a cross-sectional structure shown in Fig. 27.

[0118] Incidentally, if the fluorine or the fluorine content of the gas is too high, then the oxides are etched away during the exposure to plasma used in the present embodiment. Consequently, it is preferable that the fluorine or gas containing fluorine be a mixed gas composed of fluorides and inactive elements having, preferably, a fluorine content of 1% to 10%. The fluorides that may be used are SiF_4, BF_3, NF_3, SF_6, and gas of the fluorocarbon* series ($C_xH_yF_z$ and C_xF_y, where x, y, and z are whole numbers). As for the inactive elements, He, Ar and N_2 may be used. Moreover, the temperature of the plasma treatment was set at 400°C in the foregoing description, and it is preferable that the temperature be at 350°C or more in order to achieve the diffusion of fluorine into the gate oxide film. Moreover, in cases wherein the plasma treatment is to be carried out using fluorine after the Al alloy for the metal interconnect is formed, it is preferable that the treatment be carried out at 350°C to 440°C.

[0119] The lifetime of hot carriers was then determined for the n-type MOS transistor having a gate length of 0.5μm and a gate width of 10 μm such as the one fabricated by the manufacturing method according to the present embodiment. The determination of the lifetime of hot carriers makes it possible to evaluate the effectiveness of the manufacturing method of the present embodiment, wherein exposure to fluorine plasma or gas plasma containing fluorine is carried out and then the fluorine is diffused into the gate oxide film by subsequent heat processing. In other words, if the lifetime of hot carriers is found to be long when the MOS transistor is in operation, then this will confirm the effectiveness of the manufacturing method of the present embodiment. On the other hand, if the lifetime of hot carriers is found to be short, then there is no advantage in this method.

[0120] Moreover, the following comparison devices were used in the experiment.

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* Translator's note: a typographical error in the original assumed; the word in the original is "florocarbon".

[0121] With comparison device 1, the entire surface of the semiconductor device was exposed to plasma after sidewalls 59 had been formed, but not washed, and then a silicon oxide film 61 was formed subsequently.

[0122] With comparison device 2, after the sidewalls 59 had been formed and washed, the entire surface of the semiconductor device was exposed to fluorine plasma or gas plasma containing fluorine, and then the silicon oxide film 61 was formed.

[0123] With comparison device 3, after the silicon oxide film 61 had been formed at a low temperature, the entire surface of the semiconductor device was exposed to fluorine plasma or gas plasma containing fluorine, and then the BPSG film 62 was formed.

[0124] With comparison device 4, after the contact hole had been formed in the BPSG film 62 and the silicon film 61, the entire surface of the semiconductor device was exposed to fluorine plasma or gas plasma containing fluorine.

[0125] With comparison device 5, after the contact hole had been formed in the BPSG film 62 and the silicon oxide film 61, the entire surface of the semiconductor device was exposed to fluorine plasma or gas plasma containing fluorine.

[0126] With comparison device 6, before the interconnect 63 was formed by etching and before the resist 64 was stripped off, the entire surface of the semiconductor device was exposed to fluorine plasma or gas plasma containing fluorine, and then the resist was stripped away with an organic washing solution.

[0127] With comparison device 7, after the forming of the interconnect 63 by etching and after the stripping of the resist 64, the entire surface of the semiconductor device was exposed to fluorine plasma or gas plasma containing fluorine, and then the second interlayer film, the P-TEOS film 65, was formed without removing the fluorine.

[0128] With comparison device 8, the semiconductor device was not exposed to fluorine plasma for the purpose of improving its hot-carrier tolerance, other than the exposure carried out to form the gate, sidewalls and the contact.

[0129] The lifetime of hot carriers was determined by calculating it from the mutual conductance G_m of the n-type MOS semiconductor device in the following manner, as was the case in each of the foregoing preferred embodiments. In other words, changes in the drain electric current I_d with respect to changes in the gate voltage V_g are first measured while a drain voltage V_d of 0.1 (V) is applied. From the graph obtained by plotting the changes in the drain current against changes in the gate voltage, the maximum value G_{m0} for the mutual conductance G_m is obtained. The DC stress condition that would yield the maximum substrate current is applied on the semiconductor device for a predetermined period of time. Then, changes in the drain current I_d with respect to changes in the gate voltage V_g are again measured while a drain voltage V_d of 0.1 (V) is applied. The maximum value G_{mT} for the mutual conductance G_m is then

obtained from the results of these determinations. Then, the percentage decline in the maximum value of the mutual conductance G_m is obtained from the following equation.

[0130]

$$\{(G_{m0} - G_{mT}) / G_{m0}\} \times 100\ (\%)$$

The above determinations to obtain the percentage were repeated by varying the duration of the DC stress applied, in order to obtain the percentage decline in the maximum value of mutual conductance as a function of changes in the duration of stress applied. The graph of Fig. 28 shows the typical time dependence of $\{(G_{m0} - G_{mT}) / G_{m0}\} \times 100$. The abscissa of the graph represents the stress time (in sec.), whereas percentage (%) decline in the maximum value of the mutual conductance G_m is represented on the ordinate. Moreover, Table 2 given below shows the lifetime of hot carriers obtained for the n-type MOS semiconductor devices, comparison devices 1 to 8, where the lifetime of hot carriers was defined as $\{(G_{m0} - G_{mT}) / G_{m0}\} \times 100 = 10\%$.

[0131]

Table 2.

	Stage in the process whereat fluorine-plasma treatment is applied	Lifetime of Hot Carriers
Comparison Device 1	After the sidewalls are formed (not washed)	68,700 seconds
Comparison Device 2	After the sidewalls are formed and after washing	65,300 seconds
Comparison Device 3	After the silicon oxide film is formed at a low temperature	61,200 seconds
Comparison Device 4	After the contact hole is formed (not washed)	6,920 seconds
Comparison Device 5	After the contact hole is formed and after washing	6,780 seconds
Comparison Device 6	Before the resist is stripped	7,350 seconds
Comparison Device 7	After the resist is stripped, but before the second interlayer insulating film is formed	63,000 seconds
Comparison Device 8	Not treated with fluorine plasma	6,800 seconds

[0132] The lifetime of hot carriers of comparison device 8, which had not been treated with fluorine plasma to improve its hot-carrier tolerance, was found to be 6,800 seconds. In contrast, the lifetime of hot carriers was found to be 68,700 seconds for comparison device 1, thus confirming the effectiveness of exposure to fluorine plasma or gas plasma containing fluorine prior to washing. Moreover, the hot-carrier lifetime of the comparison device 2 was found to be 65,300 seconds, which is somewhat shorter than that of comparison device 1. This is because the residual fluorine from etching is removed by the washing carried out after the sidewalls 59 are formed. Nevertheless, it is longer than that of comparison device 8 by about ten times, and this demonstrates the effectiveness of exposure to fluorine plasma or gas plasma containing fluorine. This is because the fluorine remaining in the sidewalls 59 diffuses into the gate oxide film 55 during the formation of the silicon oxide film 61 at a low temperature, when the film is formed directly after exposure to fluorine plasma after the sidewalls 59 are washed. Therefore, improved hot-carrier tolerance is provided by the present embodiment according to the manufacturing method provided with a first feature of the present embodiment— the method wherein the sidewalls 59 are formed on the sides of the gate electrode by etching, the entire surface of the semiconductor, including the sidewalls 59, is exposed to fluorine plasma or gas

plasma containing fluorine, and then the fluorine of the fluorine layer thus formed on the sidewalls 59 is thermally diffused into the gate oxide film 55 by heat treatment without removing the fluorine layer. Moreover, improved hot-carrier tolerance is provided by the present embodiment according to the manufacturing method provided with a second feature of the present invention— the method wherein the etching residue is removed after the sidewalls 59 are formed and then the entire surface is exposed to fluorine plasma.

[0133] Moreover, the lifetime of hot carrier is 61,200 seconds for comparison device 3, in which the silicon oxide film 61 is formed at a low temperature and then exposed to fluorine plasma, and this demonstrates the effectiveness of exposure to fluorine gas plasma. Therefore, improved hot-carrier tolerance is provided by the present embodiment according to the manufacturing method provided with a third feature of the present invention— the method wherein, after the first interlayer film is formed, the entire surface is exposed to fluorine plasma or gas plasma containing fluorine, to be directly followed by a process for forming the second interlayer insulating film.

[0134] Moreover, the lifetime of hot carrier was found to be 6,920 seconds, 6,780 seconds and 7,350 second for comparison devices 4, 5 and 6, respectively, thus showing no effects of exposure to fluorine gas plasma. This is because the oxide film into which fluorine has been interfused is stripped away by washing carried out after the contact formation, by etching used to pattern the metal interconnect or by washing with an organic solvent to strip off the resist.

[0135] On the other hand, the lifetime of hot carriers was found to be 63,000 seconds for comparison product 7, wherein after the metal interconnect 63 was patterned and the resist 64 stripped, the substrate was exposed to fluorine plasma or gas plasma containing fluorine, followed directly by the forming of the P-TEOS film 65. Since this value is about ten times that obtained for comparison product 8, it demonstrates that hot-carrier tolerance can be improved with exposure to fluorine gas plasma. Therefore, improved hot-carrier tolerance is offered by the present embodiment according to the manufacturing method provided with a fourth feature of the present invention— the method in which, after the metal interconnect 63 is patterned and the resist 64 removed, the entire surface of the semiconductor is exposed to fluorine plasma or gas plasma containing fluorine, to be directly followed, without removing the fluorine, by the diffusion of fluorine into the gate oxide film 55, to terminate dangling bonds.

[0136] The foregoing preferred embodiment was described as applied to a semiconductor device having an n-type MOS transistor provided with an LDD structure, but it is also applicable to the semiconductor devices having a p-type MOS transistor or those having an MOS transistor with a single-drain structure. Moreover, the foregoing embodiment is also applicable to semiconductor devices using EEPROM, EPROM, DRAM, MOS capacitor, or GaAs or other chemical- compound semiconductors. The effects that are similar to those obtained with the foregoing embodiment are obtained in these cases.

[0137]
Advantages of the Invention: With the present invention, as described earlier, a nitrogen-laced insulating film, which is highly resistant to water permeation and virtually blocks the passage of water to the surface of the interlayer insulating film exposed between adjacent interconnects, is formed by exposing the substrate surface to gas plasma containing hydrogen after the interconnect is patterned. Consequently, at the stage where the surface of the interlayer insulating film is subjected to washing treatment carried out prior to the forming of the metal film, the nitrogen-laced insulating film is not yet formed. Therefore, the nitrogen-laced insulating film of a high resistance against water permeation is not stripped during the washing treatment. Because this insulating film is not made thinner during manufacturing, unlike in the case of the conventional method, the film can fully exhibit its original function. As a result, even when an MOS transistor is formed in the layer underlying the insulating film containing nitrogen, the diffusion of moisture into the gate oxide film of the MOS transistor is prevented by this insulating film. Consequently, the present invention provides a semiconductor device with a life expectancy that is not degraded by hot carriers when the transistor is in operation and, therefore, a semiconductor device that is durable enough to be put to practical use.

[0138] Moreover, exposing the second interlayer insulating film to gas plasma containing nitrogen results in the formation of an insulating film, which contains nitrogen and is highly resistant to water permeation, on the surface of the second interlayer insulating film. This means that the diffusion of moisture is also blocked by the nitrogen-laced insulating film formed on the second interlayer insulating film. As a result, the diffusion of moisture from the third interlayer insulating film, which is formed on the second interlayer insulating film, is blocked by two insulating films, the nitrogen-laced insulating film formed on the surface of the second interlayer insulating film and the nitrogen-laced insulating film formed on the surface of the interlayer insulating film exposed between the interconnects. As a result, when an MOS transistor is formed in the layer underlying the interlayer insulating film, the effects of moisture diffused into this MOS transistor are eliminated even more effectively.

[0139] Moreover, the semiconductor of the present invention is provided, in between the functional element and the interlayer insulating film, with a silicon oxide film, which is formed from SiH_4, N_2O and N_2 by plasma-enhanced CVD and has a hydrogen concentration of 1×10^{21} to 5×10^{22} atoms/cm^3 and a nitrogen concentration of 1×10^{21} to 2×10^{22} atoms/cm^3. This means that water that has permeated into the silicon oxide film reacts with the Si-H, Si-NH and Si-N bonds present there to produce silicon oxide. For this reason, water in the interlayer insulating films such as SOG film or O_3-TEOS film is prevented by the formation of the silicon oxide. At the same time, the drifting of hydrogen away from the silicon oxide itself is also prevented. As a result, a semiconductor device having an excellent hot-carrier tolerance can be provided. Moreover, this silicon oxide film can readily be formed by the infusion of material source gases using a flow ratio that is within the range, $SiH_4 / (N_2O + N_2) = 0.055– 0.086$.

[0140] Moreover, the forming of the interlayer insulating film by vapor deposition is carried out in a manner so that the hydrogen content supplied by Si-H bonds in the insulating film thus formed is 5×10^{20} /cm^3 or more but 5×10^{22} /cm^3 or less. This makes it possible to form an

interlayer insulating film that will provide a circuit element having excellent electrical properties.

[0141] Moreover, the interfusion of fluorine into the sidewalls by exposing the entire surface of the semiconductor substrate to fluorine plasma or gas plasma containing fluorine after the sidewalls are etched cause the fluorine to be diffused into the gate oxide film during a subsequent heat treatment. Furthermore, in instances wherein the substrate surface is washed after the sidewalls are formed, the entire surface of the semiconductor substrate is exposed to fluorine plasma or gas plasma containing fluorine in order to interfuse fluorine into the sidewalls. As a result, fluorine diffuses into the gate oxide film during the subsequent heat treatment. This diffusion of fluorine into the gate oxide film results in the termination of silicon dangling bonds with fluorine. Therefore, a semiconductor device having an excellent hot-carrier tolerance is provided.

[0142] Furthermore, exposing the surface of the interlayer insulating film to fluorine plasma or gas plasma containing fluorine causes the diffusion of fluorine into the gate oxide film during the subsequent heat treatment.

[0143] Moreover, if the interconnect is to be formed after the interlayer insulating film and the contact hole are formed, then the entire surface of the semiconductor substrate is exposed to fluorine plasma or gas plasma containing fluorine after the resist is removed. Fluorine is then diffused into the gate oxide film by carrying out the next step in the sequence without removing the fluorine of the interlayer insulating film. These steps also provide a semiconductor device having an excellent hot-carrier tolerance.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional view of a semiconductor device obtained by the manufacturing method according to a first embodiment of the present invention.

Fig. 2 is a cross-sectional view illustrating the first step of the manufacturing method according to the first embodiment.

Fig. 3 is a cross-sectional view illustrating the second step of the manufacturing method according to the fist embodiment.

Fig. 4 is cross-sectional view illustrating the third step of the manufacturing method according to the first embodiment.

Fig. 5 is a cross-sectional view illustrating the fourth step of the manufacturing method according to the fist embodiment.

Fig. 6 is s graph profiling changes in the mutual conductance with respect to the duration of DC stress applied obtained for semiconductor devices manufactured according to the method of the first embodiment and for comparison devices manufactured by other methods.

Fig. 7 is a cross-sectional view of the fist step of the manufacturing method according to a second embodiment of the present invention.

Fig. 8 is a cross-sectional view of the second step of the manufacturing method according to the second embodiment.

Fig. 9 is a cross-sectional view of a semiconductor device according to the second embodiment.

Fig. 10 is a graph showing the results of the FTIR determination carried out to analyze the reaction of water in the P-SiO film according to the second embodiment.

Fig. 11 is a graph showing the results of the determination of the resistance to heavy-water permeation of P-SiO films formed using varied flow ratios of gases used as the material source.

Fig. 12 is a cross-sectional view illustrating the constitution of a semiconductor device having a single-level metal interconnect structure used to compare the lifetime of hot carriers with that of the semiconductor device according to the second embodiment.

Fig. 13 is a graph showing the changes in the percentage decline of the maximum value for the mutual conductance with changes in the duration of stress obtained for the semiconductor device according to the second embodiment and for various semiconductor devices manufactured according to methods other than the second embodiment.

Fig. 14 is a graph showing changes in the lifetime of hot carriers with respect to changes in the flow rate of gases used as the material source according to the second embodiment.

Fig. 15 is a graph showing changes in the nitrogen and hydrogen concentrations with respect to changes in the flow ratio of gases used as the material source according to the second embodiment.

Fig. 16 is a schematic drawing illustrating a section of a plasma CVD apparatus used in the method of forming the interlayer insulating film according to a third embodiment of the present invention.

Fig. 17 is a graph showing the relationship between the concentration of hydrogen of the Si-H bonds present in the film and the film-formation rate according to the third embodiment.

Fig. 18 is a graph showing the relationship between the Si/O ratio of the P-SiO film and the hydrogen content supplied by Si-H bonds in the film according to the third embodiment.

Fig. 19 is a graph showing the relationship between the concentration of deuterium and the depth from the surface of the P-SiO film according to the third embodiment.

Fig. 20 is a cross-sectional view of a semiconductor device manufactured according to the manufacturing method of the third embodiment.

Fig. 21 is a graph showing changes in the percentage decline in the maximum value of the mutual conductance with changes in the duration of stress applied obtained for the semiconductor devices according to the third embodiment and various semiconductor devices manufactured according to other methods.

Fig. 22 is a cross-sectional view illustrating the first step of the method of manufacturing a semiconductor device according to a fourth embodiment of the present invention.

Fig. 23 is a cross-sectional view illustrating the second step of the method of manufacturing a semiconductor device according to the fourth embodiment.

Fig. 24 is a cross-sectional view illustrating the third step of the method of manufacturing a semiconductor device according to the fourth embodiment.

Fig. 25 is cross-sectional view illustrating the fourth step of the method of manufacturing a semiconductor device according to the fourth embodiment.

Fig. 26 is a cross-sectional view illustrating the fifth step of the method of manufacturing a semiconductor device according to the fourth embodiment.

Fig. 27 is a cross-sectional view of a semiconductor device obtained by the manufacturing method according to the fourth embodiment.

Fig. 28 is a graph showing changes in the percentage decline in the maximum value of the mutual conductance with changes in the duration of stress applied obtained for the semiconductor devices manufactured according to the fourth embodiment and for various semiconductor devices manufactured according to other methods.

Description of the Reference Numerals

1	p-type silicon semiconductor substrate
2	p-well
3	channel stopper
4	element-isolation silicon oxide film
5	gate oxide film
6	polysilicon
7	tungsten silicide film
8	sidewall
9	silicon oxide film
10	silicon oxide film containing phosphorus and boron (BPSG)
11 & 18	metal interconnects
12 & 14	nitrogen-laced insulating film
13 & 17	P-TEOS film
15	O_3-TEOS film
16	SOG film
19	phosphorus-doped silicon oxide film
20	passivation film
21	P-SiO film

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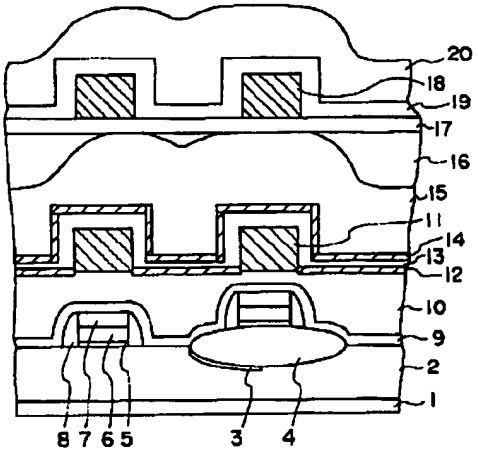
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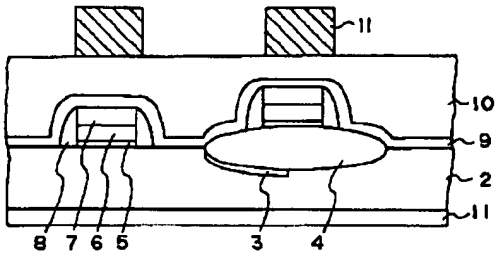
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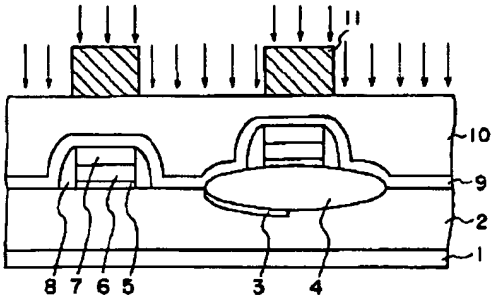
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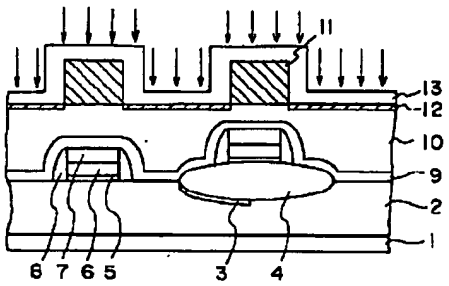
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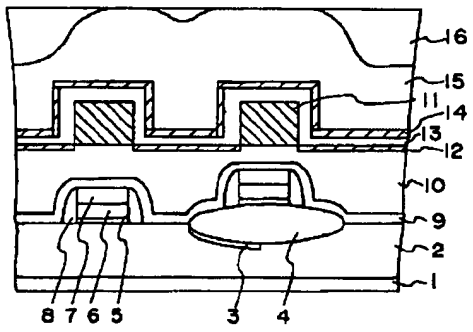
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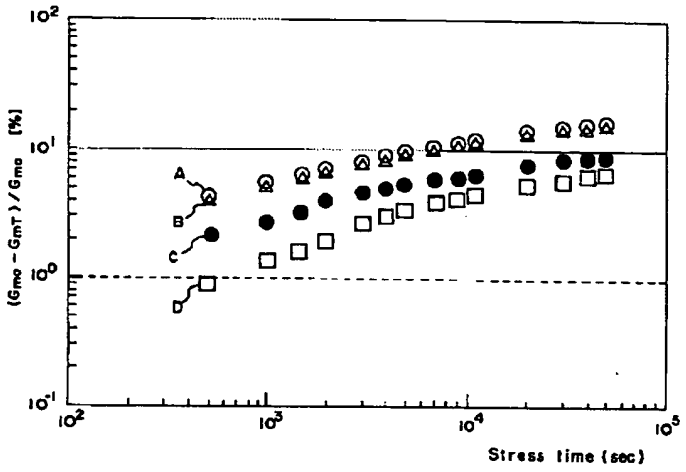

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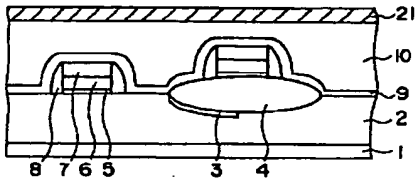

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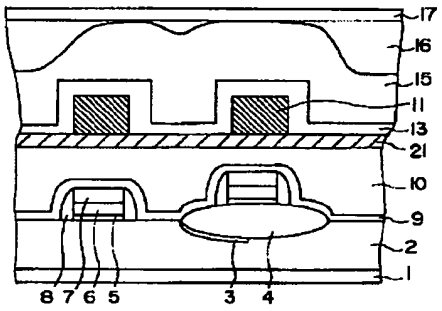

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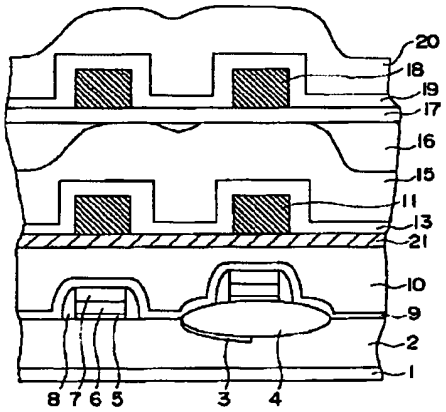

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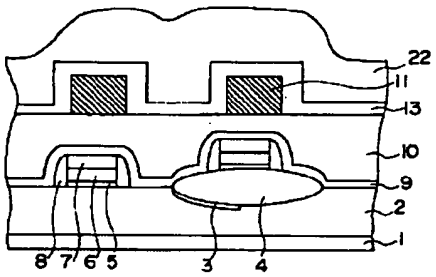

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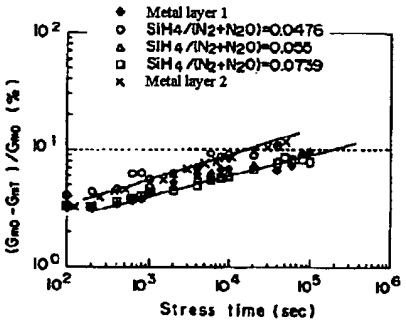

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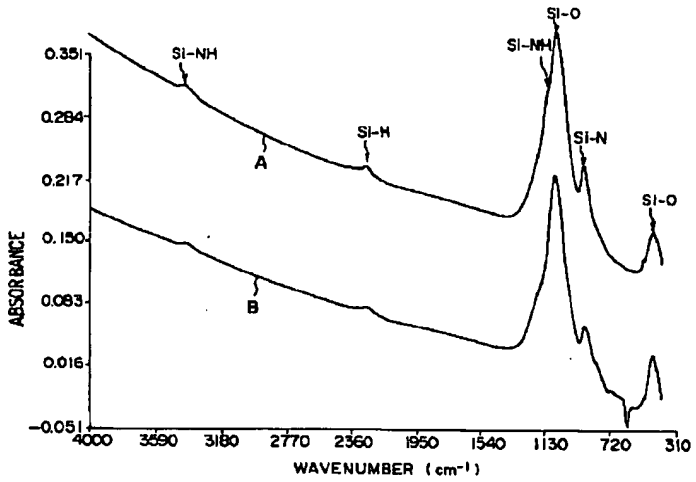

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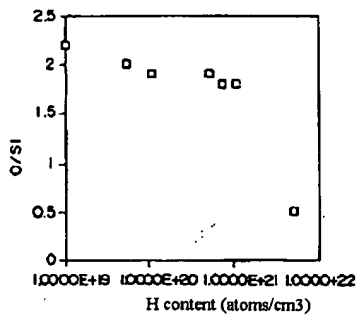

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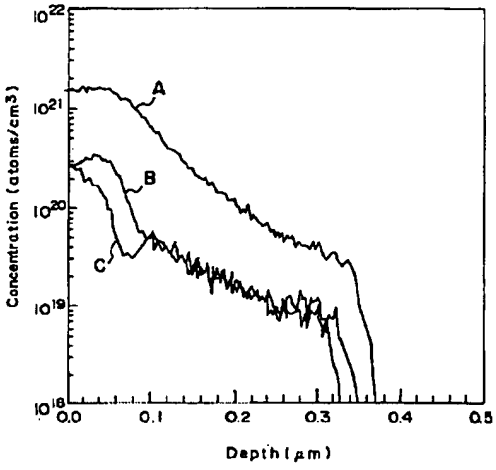

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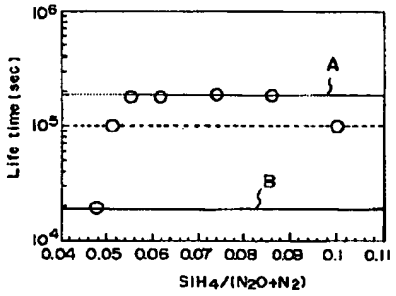

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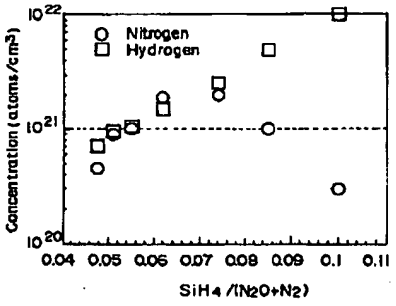

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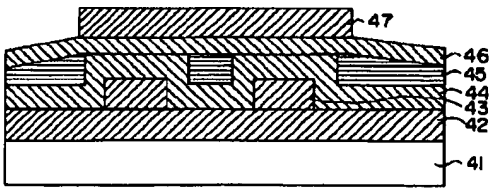

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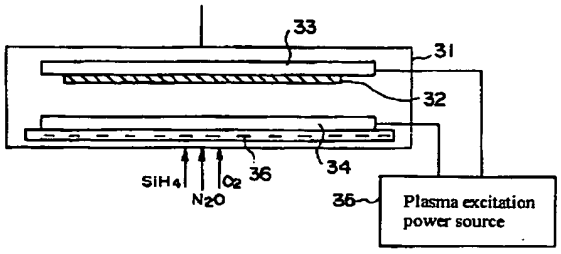

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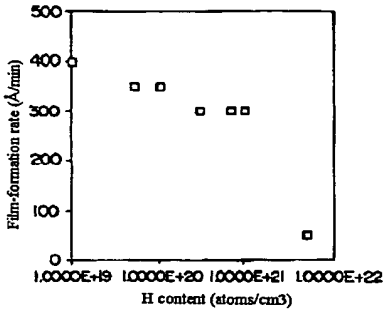

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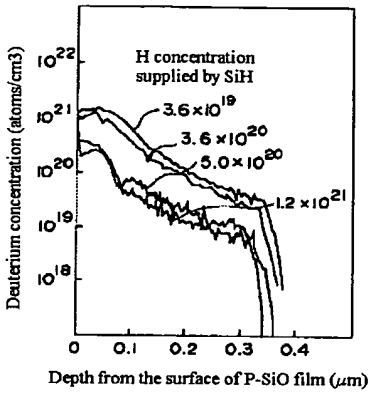

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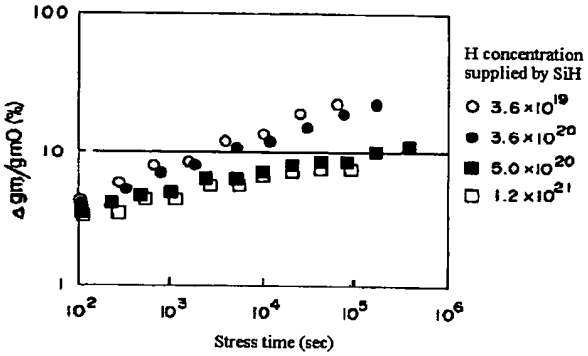

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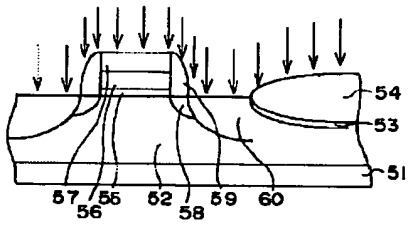

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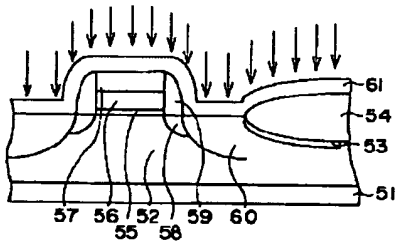

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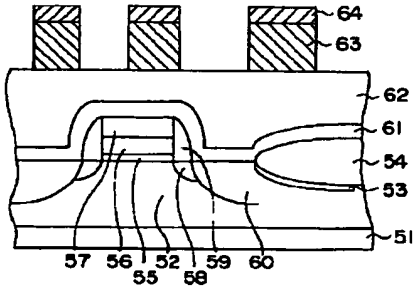

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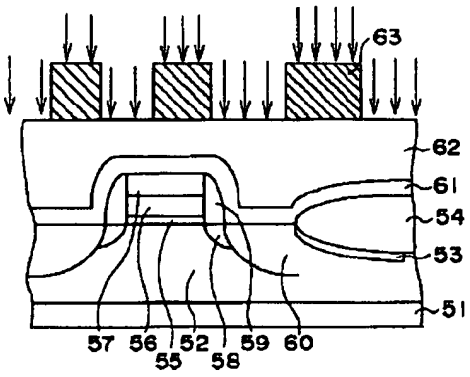

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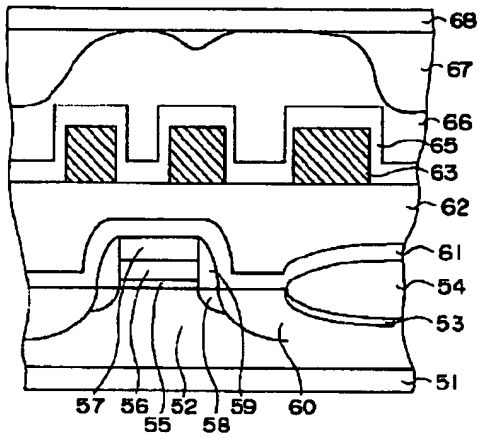

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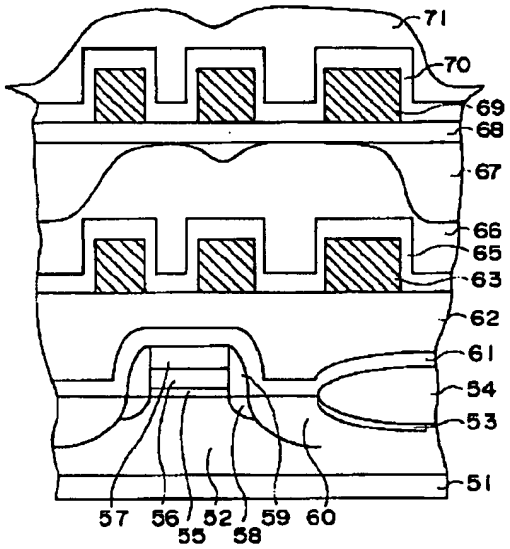

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